S845WD1-E Server Board

Technical Product Specification

Intel order number A93850-003

Revision 3.0

January 2003

Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
May 2002	1.0	Initial Release.
Dec 2002	2.0	Updated with S845WD1H information, corrected video memory, minor corrections to BIOS tables, added errata appendix.
Jan 2003	3.0	Minor updates to add support web site information.

This product specification applies to the Intel® Server Board S845WD1-E with BIOS identifier WD84510A.86B.

Changes to this specification will be published in the Intel Server Board S845WD1-E Specification Update before being incorporated into a revision of this document.

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1. Introduction

The S845WD1-E Technical Product Specification (TPS) provides a high level technical description for the Intel® S845WD1-E Server Board. It details the architecture and feature set for all functional sub-systems that make up the server board.

This TPS covers all S845WD1-E server boards, which include the following product codes: S845WD1, S845WD11U and S845WD1H. When appropriate, specific product codes are used to relay important information that pertains to that version of the S845WD1-E server board only.

This document is divided into the following main categories:

Chapter 2: Server Board Overview

Chapter 3: Functional Architecture

Chapter 4: Technical Reference

Chapter 5: Connectors and Jumper Blocks

Chapter 6: Overview of BIOS Features

Chapter 7: BIOS Setup Program

Chapter 8: Error Reporting and Handling

Chapter 9: General Specifications

2. Server Board Overview

2.1 S845WD1-E Feature Set

The S845WD1-E server board provides an embedded ATA-100* "Valu-Raid" interface and supports the following feature set:

- Support for an Intel® Celeron® processor in a µPGA478 socket
- Support for an Intel® Pentium® 4 processor in a µPGA478 socket
- Support for an Intel® Pentium® 4 processor with hyper-threading technology when using the S845WD1H board only.

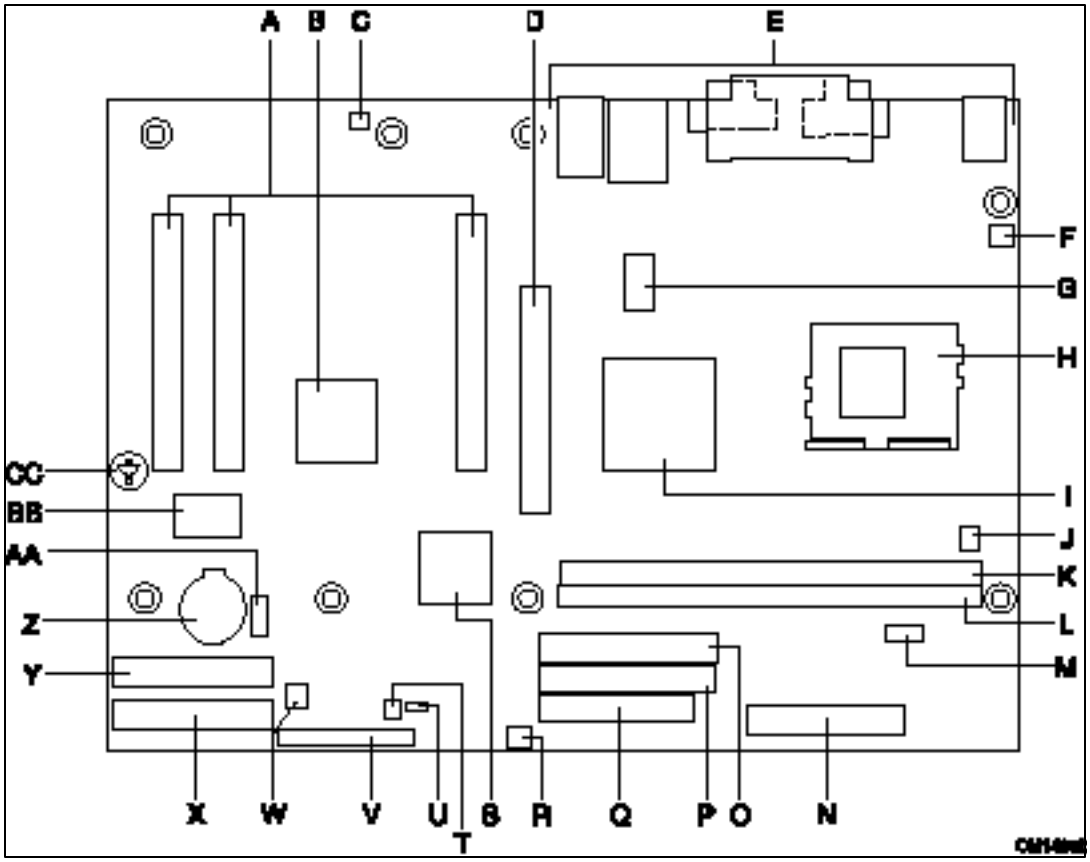
NOTE

Due to the increased thermal requirements of hyper-threading processors, the S845WD1H server board is not intended for use in a 1U form factor chassis. The S845WD11U server board is intended for use in a 1U form factor chassis and only supports up to 2.8GHz processors without hyper-threading due to thermal requirements in a 1U chassis and the thermal capabilities of the active-fan heat sink provided. If you require a 1U chassis implementation, please use the S845WD11U server board.

- 400/533 MHz System Bus
- Intel® 845E chipset
  - Intel® 82845E Memory Controller Hub (MCH)
  - Intel® 82801BA I/O Controller Hub (ICH2)
  - Intel® 82802AB 4 Megabit Firmware Hub (FWH)
- Support for single-sided or double-sided DIMMs (DDR 200 and DDR 266) providing up to 2 GB system memory with two 184-pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets.
- One AGP bus with AGP connector:
  - One AGP connector supporting 1.5 V 4X AGP cards
- One independent PCI bus (32-bit, 33 MHz, 5 V) with three PCI connectors and four embedded devices:
  - 2D/3D graphics controller: ATI Rage* XL Video Controller with 8 MB of SDRAM
  - Two Intel10/100 82550PM Fast Ethernet Controllers
  - ATA-100 controller: Promise Technology* PDC20267
- LPC (Low Pin Count) bus segment with one embedded device:
  - SMSC LPC47M102 LPC Bus I/O controller controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse)
- X-Bus segment with one embedded device:
  - Flash ROM device for system BIOS: Intel 32 megabit 28F320C3 Flash ROM

- Two external Universal Serial Bus (USB) ports with an additional internal header providing two optional USB ports for front panel support
- One serial port and one serial port header.
- One parallel port.
- Two IDE interfaces with UDMA 33, ATA-66/100 support
- Support for up to three system fans and one processor fan
- Server System Infrastructure (SSI)-compliant connectors for SSI interface support: front panel, power connector
- Hardware Monitor Subsystem:
  - Voltage sense to detect out of range power supply voltages
  - Thermal sense to detect out of range thermal values
  - Four fan sense inputs used to monitor fan activity

The figure below shows the functional blocks of the server board and the plug-in modules that it supports.



A. PCI expansion slots	B. ATI Rage XL Video Controller
C. Chassis intrusion connector	D. AGP connector
E. Back panel connectors	F. System fan (fan 2)
G. 12 V auxiliary power connector	H. µPGA478 processor socket
I. Intel 82845E memory controller hub (MCH)	J. Chassis fan
K. DIMM2 socket	L. DIMM1 socket
M. Serial port B connector	N. Main power connector
O. Secondary IDE connector	P. Primary IDE connector
Q. Floppy drive connector	R. System fan (fan 3)
S. Intel 82801BA I/O controller hub (ICH2)	T. HDD LED connector
U. Configuration jumper block	V. Front panel header
W. System fan (fan 1)	X. Primary RAID IDE connector
Y. Secondary RAID IDE connector	Z. Battery
AA. Front panel USB connector	BB. Promise ATA RAID controller
CC. Speaker	

Figure 1. S845WD1-E Server Board Diagram

3. Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the S845WD1-E server board.

3.1 Processor and Memory Subsystem

The Intel 82845E Memory Controller Hub (MCH) is one component of the Intel 845E chipset. The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface.

3.1.1 Processor Support

The S845WD1-E server board supports a single Pentium 4 or Celeron processor (in a µPGA478 socket) with a system bus of 400 /533 MHz. The S845WD1 and S845WD11U server boards support the processors listed in Table 1. The S845WD1H server board supports the processors listed in Table 2.

Table 1. S845WD1, S845WD11U Processor Support Matrix

Type	Designation	System Bus	L2 Cache Size
Celeron® processor	1.8 and 1.9 GHz	400 MHz	128 KB
Pentium® 4 processor	1.8, 2.0, 2.26, 2.4, 2.53, 2.6, 2.66, and 2.8 GHz	400 / 533 MHz	512 KB

Table 2. S845WD1H Processor Support Matrix

Type	Designation	System Bus	L2 Cache Size
Celeron® processor	1.8 and 1.9 GHz	400 MHz	128 KB
Pentium® 4 processor	1.8, 2.0, 2.26, 2.4, 2.53, 2.6, 2.66, and 2.8 GHz	400 / 533 MHz	512 KB
Pentium® 4 processor with hyper-threading technology	3.06GHz	533 MHz	512 KB

CAUTION

Use only the processors listed above. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Server Board S845WD1-E Specification Update or go to http://support.intel.com/support/motherboards/server/s845wd1-e/ for the most up-to-date list of supported processors for this board.

NOTE

Use only ATX12V or EPS12V compliant power supplies with the S845WD1-E server board. ATX12V and EPS12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. Always connect the 20-pin (or 24-pin) and 4-pin (or 8-pin) leads of ATX12V or EPS12V power supplies to the corresponding connectors on the S845WD1-E server board, otherwise the board will not boot.

Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

3.1.1.1 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc. through the CPUID instruction. The requirement is for the processor to run at a fixed speed. The processor cannot be programmed to operate at a lower or higher speed.

On the S845WD1-E platform, the BIOS is responsible for configuring the processor speed. The BIOS uses CMOS settings to determine which speed to program into the speed setting device. The processor information is read at every system power-on.

3.1.2 Memory Subsystem

The S845WD1-E server board provides two DIMM slots and supports a maximum memory capacity of 2 GB. The DIMM organization is x72 which includes eight ECC check bits. ECC from the DIMMs are passed through to the processor's front side bus. Memory scrubbing, single-bit error correction and multiple-bit error detection is supported. Memory can be implemented with either single-sided (one row) or double-sided (two row) DIMMs.

NOTE

Remove the AGP video card before installing or upgrading memory to avoid interference with the memory retention mechanism.

NOTE

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

NOTE

For ECC functionality, all installed DIMMs must be ECC. If both ECC and non-ECC DIMMs are used, ECC will not function.

NOTE

Only low profile DIMMs can be supported in a 1U server chassis.

The smallest supported DIMM size is 64 MB. The largest size DIMM supported is a 2-GB stacked un-buffered DDR200/266 ECC DIMM based on 512-megabit technology. See the table below for supported memory configurations.

Table 3. Supported Memory Configurations

DIMM Capacity	Number of Sides	DDR SDRAM Density	DDR SDRAM Organization Front-side/Back-side	Number of DDR SDRAM Devices
64 MB	SS	64 Megabit	8 M x 8/empty	8
64 MB	SS	128 Megabit	8 M x 16/empty	4
128 MB	DS	64 Megabit	8 M x 8/8 M x 8	16 (Note 1)
128 MB	SS	128 Megabit	16 M x 8/empty	8
128 MB	SS	256 Megabit	16 M x 16/empty	4
256 MB	DS	128 Megabit	16 M x 8/16 M x 8	16 (Notes 1 and 2)
256 MB	SS	256 Megabit	32 M x 8/empty	8
256 MB	SS	512 Megabit	32 M X 16/empty	4
512 MB	DS	256 Megabit	32 M x 8/32 M x 8	16 (Notes 1 and 2)
512 MB	SS	512 Megabit	64 M X 8/empty	8
1024 MB	DS	512 Megabit	64 M X 8/64 M X8	16 (Notes 1 and 2)

Notes:

1. If the number of DDR SDRAM devices is greater than nine, the DIMM will be double sided.
2. Front side population/back side population indicated for DDR SDRAM density and DDR SDRAM organization.

In the second column, “DS” refers to double-sided memory modules (containing two rows of DDR SDRAM) and “SS” refers to single-sided memory modules (containing one row of DDR SDRAM).

DIMM and memory configurations must adhere to the following:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered single-sided or double-sided DIMMs
- Maximum total system memory: 2 GB; Minimum total system memory: 64 MB
- 200/266 MHz DDR SDRAM DIMMs only
- Serial Presence Detect (SPD)

- Non-ECC and ECC DIMMs

Only DIMMs tested and qualified by Intel or a designated memory test vendor will be supported on the S845WD1-E server board. A list of qualified DIMMs will be made available through http://support.intel.com/support/motherboards/server/s845wd1-e/. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.

The S845WD1-E Server Board has been designed to support DIMMs based on 512 Megabit technology for a maximum on-board capacity of up to 2 GB, but this technology has not been validated on this board.

3.2 Intel® 845E Chipset

The Intel 845E chipset consists of the following devices:

- Intel 82845E Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801BA I/O Controller Hub (ICH2) with AHA bus
- Intel® 82802AB Firmware Hub (FWH)

The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH2 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 2.

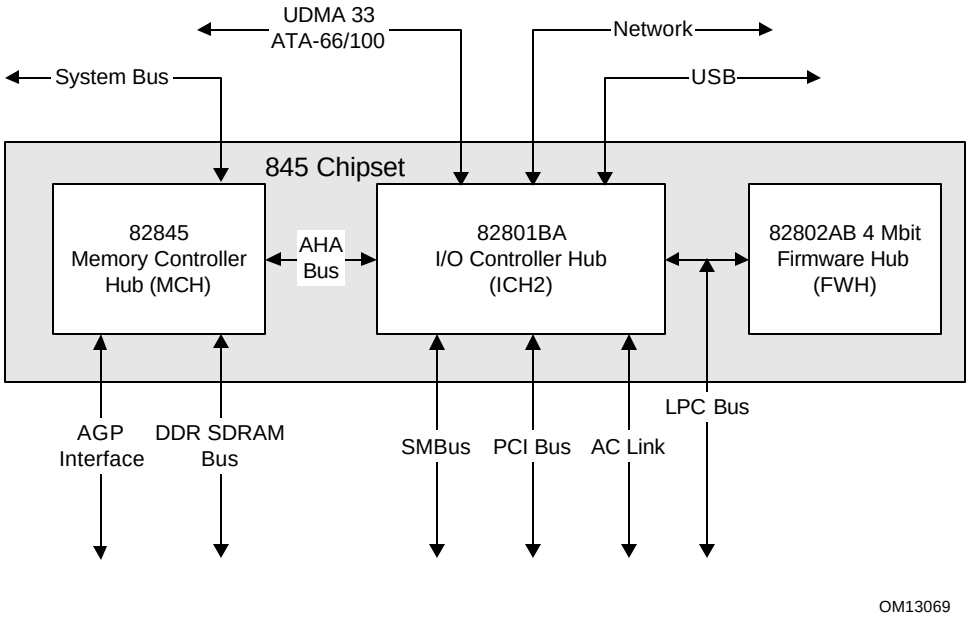


Figure 2. Intel 845E Chipset Block Diagram

For information about	Refer to
The Intel 845E chipset	http://developer.intel.com
Resources used by the chipset	Chapter 2

3.2.1 AGP

The AGP connector supports AGP add-in cards with 1.5 V Switching Voltage Level (SVL).

For information about	Refer to
The AGP connector	Section 5.3

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.2, AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

3.2.2 USB

The S845WD1-E server board has four USB 1.1 ports; one USB peripheral can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. Two of the USB ports are implemented with stacked back panel connectors; the other two are accessible via the front panel USB connector at J8G1. The S845WD1-E server board fully supports UHCI and uses UHCI-compatible software drivers.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 1
The location of the front panel USB connector	Figure 1
The signal names of the front panel USB header	Section 5.8
Legacy USB support	Section 6.4

Wake from USB	Section 3.6.2.6

3.2.3 IDE Interfaces

The ICH2's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2's ATA-100 logic can achieve transfer rates up to 100 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 7.3.4.1.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The S845WD1-E server board supports Laser Servo (LS-120) diskette technology through the IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 1
The signal names of the IDE connectors	Table 25
BIOS Setup program's Boot menu	Table 50
IDE Configuration Submenu	Section 7.3.4

3.2.3.1 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows an add-in SCSI controller to use the same LED as the on-board IDE controller. For proper operation, this connector should be wired to the LED output of the add-in SCSI controller. The LED indicates when data is being read from, or written to, both the add-in SCSI controller and the IDE controller.

For information about	Refer to
The location of the SCSI hard drive activity LED connector	Figure 1

3.2.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock provides a time-of-day clock and a multi-century calendar with alarm features. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

3.2.5 Intel® 82802AB 4 Megabit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS program
- Logic that enables protection for storing and updating of platform information

3.3 I/O Controller

The SMSC* LPC47M102 I/O Controller provides the following features:

- Low pin count (LPC) interface
- 3.3 V operation
- One serial port connector and one serial port header
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support

- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for two 1.2 MB, 1.44 MB, or 2.88 MB diskette drives
- Intelligent power management, including a programmable wake up event interface
- PCI power management support
- Fan control:
  - Four fan control outputs
  - Four fan tachometer inputs

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M102 I/O controller	http://www.smsc.com

3.3.1 Serial Ports

The S845WD1-E server board has one 9-pin D-sub serial port connector and one 2 x 5 serial port connector. The serial port A connector is located on the back panel. The serial port B connector is located near the main power connector. The serial ports' NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the serial port A connector	Figure 1
The signal names of the serial port A connector	Table 28
The location of the serial port B connector	Figure 1
The signal names of the serial port B header	Table 29

3.3.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. In the BIOS Setup program, the parallel port can be set to the following modes:

- Output only (PC AT*-compatible mode)
- Bi-directional (PS/2* compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 1
Setting the parallel port's mode	Table 42

3.3.3 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

For information about	Refer to
The location of the diskette drive connector	Figure 1
The signal names of the diskette drive connector	5.9
The supported diskette drive capacities and sizes	Table 45

3.3.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch* circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI* keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 1
The signal names of the keyboard and mouse connectors	Table 30

3.4 Hardware Management Subsystem

The hardware management features enable the S845WD1-E server board to be compatible with the Wired for Management (WfM) specification 2.0. The server board complies with DMI specification 2.0 and has several hardware management features, including the following:

- Fan monitoring
- Thermal and voltage monitoring
- Chassis intrusion detection

3.4.1 Hardware Monitor Component

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing

- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12V, +5 V, +3.3 V, +1.5 V, 3.3 VSB, and Vccp) to detect levels above or below acceptable values
- SMBus interface

3.4.2 Fan Monitoring

The Hardware Management ASIC provides four fan tachometer inputs. Monitoring can be implemented using LANDesk™ Client Manager or third-party software.

For information about	Refer to
The functions of the fan connectors	Section 3.6.2.2
The location of the fan connectors	Figure 1
The signal names of the fan connectors	Section 5.12.1

3.4.3 Chassis Intrusion and Detection

The S845WD1-E server board supports a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed the mechanical switch is in the closed position.

For information about	Refer to
The location of the chassis intrusion connector	Figure 1

NOTE

Chassis intrusion detection may be implemented using Intel® LANDesk™ Client Manager or third-party software.

3.5 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices

- Power Management Event (PME#) wake-up support

3.6 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the S845WD1-E server board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in board (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 6)
- Support for a front panel power and sleep mode switch

Table 4 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 4. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

For information about	Refer to
The S845WD1-E server board' compliance level with ACPI	Section 3.6

3.6.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put

the system as a whole into a low-power state. The S845WD1-E server board supports sleep states S0, S1, S3, S4 and S5.

Table 5. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

3.6.1.2 Wake-up Devices and Events

Table 6 lists the devices or specific events that can wake the computer from specific states.

Table 6. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S4, S5
RTC alarm	S1, S3, S4, S5
LAN	S1, S3, S4, S5 (Note 1)
PME#	S1, S3, S4, S5
Modem (back panel Serial Port A)	S1, S3

USB	S1, S3

Notes:

1. For LAN and PME#, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

3.6.1.3 Plug and Play

In addition to power management, ACPI provides control information so that operating systems can facilitate Plug and Play. ACPI is used only to configure devices that do not use other hardware configuration standards. PCI devices for example, are not configured by ACPI.

3.6.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 9.2 for additional information.

The S845WD1-E server board provides several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

3.6.2.1 Power Connector

ATX12V or EPS12V compliant power supplies and the S845WD1-E server board can turn off the system power through software control. When the system receives the correct command from the operating system, the power supply removes non-standby voltages from the system.

When power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the After Power Failure in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 1
The signal names of the power connector	Section 5.1
The BIOS Setup program's Boot menu	Table 50

3.6.2.2 Fan Connectors

Table 7 summarizes the function/operation of the fan connectors.

Table 7. Fan Connector Function/Operation

Connector	Description
Processor fan (CPU FAN)	• +12 V DC connection for a processor fan or active fan heatsink. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S4 or S5 state. • Wired to a fan tachometer input of the SMSC LPC47M102 I/O controller. (routed to Hardware Management ASIC)
Front chassis fan (FAN1)	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S4 or S5 state. • Wired to a fan tachometer input of the Hardware Management ASIC.
Rear chassis fans (FAN2 and FAN3)	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S4 or S5 state. • Wired to a fan tachometer input of the Hardware Management ASIC.

For information about	Refer to
The location of the fan connectors	Figure 1
The signal names of the fan connectors	Table 31

3.6.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the 5V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply. Refer to Section 9.2 for additional information.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the S845WD1-E server board supports LAN wake capabilities with ACPI in the following ways:

- The PCI bus PME# signal for PCI 2.2 compliant LAN designs
- The on-board LAN subsystem

3.6.2.4 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5V standby line for the power supply must be capable of providing adequate +5V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply. Refer to Section 9.2 for additional information.

Instantly Available PC technology enables the S845WD1-E server board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is off.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 6

The S845WD1-E server board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that support this specification can participate in power management and can be used to wake the computer.
The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

The standby power indicator LED (CR3G1) shows that power is still present even when the computer appears to be off. Figure 3 shows the location of the standby power indicator LED.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

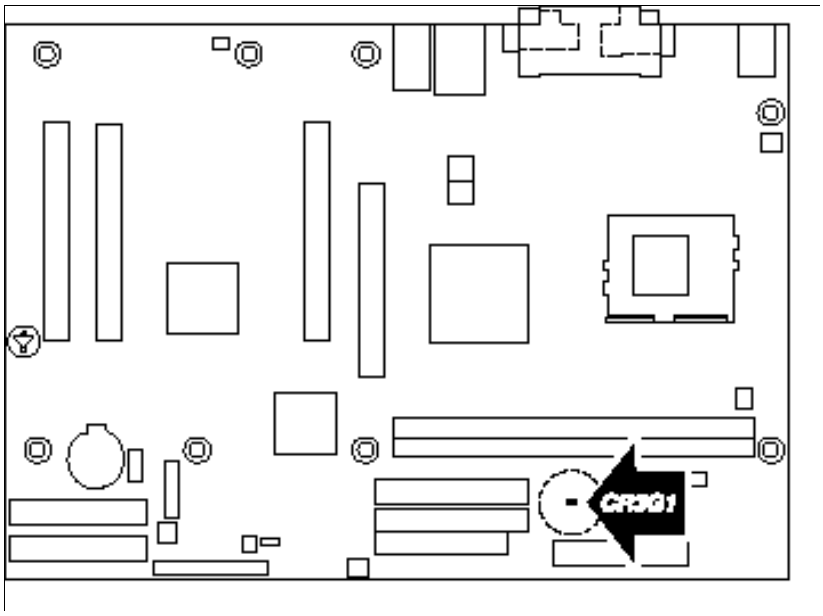


Figure 3. Location of the Standby Power Indicator LED (CR3G1)

3.6.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

3.6.2.6 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

3.6.2.7 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

3.6.2.8 PME# Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

3.7 Clock Generation and Distribution

All buses on the S845WD1-E baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100/133-MHz at 2.5 V & 3.3 V logic levels: For the mPGA478 socket, the MCH, and the ITP port.
- 66 MHz at 3.3 V logic levels: For the MCH, RAID controller and the AGP clocks.
- 33.3 MHz at 3.3 V logic levels: For the PCI slots and devices.
- 14.318 MHz at 3.3V logic levels: ICH2 and Super I/O clocks.

The synchronous clock sources on the S845WD1-E baseboard are:

- 100/133-MHz host clock generator for processor, MCH, Memory DIMMs, and the ITP.
- 66-MHz clock for MCH, RAID controller and the AGP clocks.
- 48-MHz clock for USB.
- 33.3-MHz PCI reference clock.
- 14.318 MHz ICH2 and Super I/O clocks.

The S845WD1-E baseboard also provides asynchronous clock generators:

- 25-MHz clocks for the embedded network interface controllers.
- 29.4989-MHz clock for the embedded video controller.
- 32-KHz clock for the RTC.

3.8 PCI I/O Subsystem

The primary I/O bus for the S845WD1-E server board is PCI, with one independent PCI bus. The PCI bus complies with the *PCI Local Bus Specification, Rev 2.2*. The PCI bus is directed through the Intel 82801BA I/O Controller Hub (ICH2). The table below lists the characteristics of the PCI bus.

Table 8. PCI Bus Characteristics

Voltage	Width	Speed	Type	Comments
5 V	32-bits	33 MHz	Independent Bus	Supports full-length cards

3.8.1 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O for the S845WD1-E server board is directed through the Intel 82801BA I/O Controller Hub (ICH2). The PCI bus supports the following embedded devices and connectors:

- 2D/3D Graphics Accelerator: ATI Rage XL Video Controller.
- Two 10/100 Network Interface Controllers: Intel 82550PM Fast Ethernet Controller.
- ATA-100 controller: Promise Technology PDC20267.
- Two Ultra DMA 33 / ATA 66/100 connectors.

Each of the embedded devices listed above, with exception to the Ultra DMA 33 / ATA 66/100 connectors, will be allocated a GPIO to disable the device.

3.8.1.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows each IDSEL value for the PCI bus devices and the corresponding device description.

Table 9. PCI Bus Configuration IDs

IDSEL Value	Device
25	PCI slot 1 (closest to AGP connector)
26	PCI slot 2 (middle slot)
27	PCI slot 3 (closest to left edge of board)
28	Intel® 82550PM Fast Ethernet Controller
29	Intel® 82550PM Fast Ethernet Controller
30	ATA-100* controller Promise Technology* PDC20267
31	ATI Rage* XL Video Controller

3.8.1.2 PCI Arbitration

The PCI bus supports six PCI masters (ATI Rage XL, two Intel® 82550 chips, Promise ATA-100 Controller, PCI connector 1 and an arbiter (PCI connector 2 and PCI connector 3). All PCI masters must arbitrate for PCI access, using resources supplied by the ICH2. The host bridge PCI interface (ICH2) arbitration lines REQx and GNTx are a special case in that they are internal to the host bridge.

3.8.2 ATA-100

The S845WD1-E server board provides an embedded dual channel ATA-100 bus through the use of the Promise Technology PDC20267 ASIC. The PDC20267 ATA-100 controller contains two independent ATA-100 channels that share a single 32-bit, 33-MHz PCI bus master interface as a multifunction device, packaged in a 128-pin PQFP.

The ATA-100 controller supports the following features:

- The scatter / gather mechanism supports both Direct Memory Access (DMA) and Programmable I/O (PIO) IDE drives.
- Support for ATA PIO Mode 0, 1, 2, 3, 4, DMA Mode 0, 1, 2, and Ultra DMA Mode 0, 1, 2, 3, 4, 5.
- The IDE drive transfer rate is capable of up to 100 MB/sec per channel.
- The host interface complies with *PCI Local Bus Specification Revision 2.2*.
- 32-bit, 33-MHz bus speed and 132 MB/sec sustained transfer rate.

The Promise* PDC20267 supports IDE RAID through dual ATA-100 Channels. In a RAID configuration, multiple IDE hard drives are placed into one or more arrays of disks. Each array is seen as an independent disk, though the array may include upwards of two, three, or four drives. The IDE RAID can be configured as followings:

- RAID 0: Striping one to four drives.
- RAID 1: Mirroring two drives.
- RAID 1 +: Spare drive (three drives).
- RAID 0 +: One to four drives are required.

RAID 0 configurations are used for high-performance applications, as it doubles the sustained transfer rate of its drives. RAID 1 configurations primarily used for data protection. It creates an identical drive backup to a secondary drive. Whenever a disk write is performed, the controller sends data simultaneously to a second drive located on a different data channel. With four drives attached to dual ATA-100 channels, two striped drive pairs can mirror each other (RAID 0+1) for storage capacity and data redundancy.

3.8.3 Video Controller

The S845WD1-E server board provides an ATI Rage XL PCI graphics accelerator, along with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

The S845WD1-E server board provides a standard 15-pin VGA connector and supports disabling of the on-board video through the BIOS Setup menu or when a plug-in video card is installed in the AGP slot or any of the PCI slots.

3.8.3.1 Video Modes

The Rage XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD, as well as various display resolution, refresh rates, and color depths.

Table 10. Video Modes

2D Mode	Refresh Rate (Hz)	S845WD1-E 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**S845WD1-E 3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**S845WD1-E 3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

3.8.3.2 Video Memory Interface

The memory controller subsystem of the Rage XL arbitrates requests from direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The S845WD1-E supports an 8 MB SDRAM device for video memory.

3.8.4 Network Interface Controller (NIC)

The S845WD1-E server board supports two 10Base-T/100Base-TX Network Interface Controllers (NICs) based on the Intel 82550PM NIC. The 82550PM is a highly integrated PCI LAN controller in a thin BGA 15mm package. The controller's baseline functionality is equivalent to that of the Intel 82559, with the addition of Alert-on-LAN functionality. The S845WD1-E server board supports independent disabling of the two NIC controllers using the BIOS Setup menu.

The 82550PM supports the following features:

- Glueless 32-bit PCI, CardBus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2.*
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY.
- IEEE 820.3u auto-negotiation support.
- Full duplex support at both 10 Mbps and 100 Mbps operation.
- Integrated UNDI ROM support.
- MDI/MDI-X and HWI support.
- Low power +3.3 V device.

NOTE

It is recommended that if cable lengths in excess of approximately 70m are required, that the cables used are rated for insertion loss of .075dB/m or less. Customers using cables in excess of 100m may see some degradation of performance.

3.8.4.1 NIC Connector and Status LEDs

The 82550 drives two LEDs located on each network interface connector. The amber LED indicates network connection when on, and transmit/receive activity when blinking. The yellow LED indicates 100-Mbps operation when lit, and 10-Mbps when off.

4. Maps and Interrupts

In this section, Table 11 describes the system memory map, Table 12 shows the I/O map, Table 13 lists the DMA channels, Table 14 defines the PCI configuration space map, and Table 15 describes the interrupts.

4.1 Memory Map

Table 11. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 2097152 K	100000 - 7FFFFFFF	2047 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

4.2 I/O Map

Table 12. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS/Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	APM control
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel

Address (hex)	Size	Description
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4/video (8514A)
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82845 MCH
03C0 - 03DF	32 bytes	Intel 82845 MCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5 0370 - 0375	6 bytes 6 bytes	Diskette channel 1 Diskette channel 2
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

Address (hex)	Description
8 bytes on an 8-byte boundary	Unknown
96 contiguous bytes starting on a 128-byte divisible boundary	ICH2 (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary	S845WD1-E server board resource
32 contiguous bytes starting on a 32-byte divisible boundary (Note 5)	ICH2 (USB controller 1)
16 contiguous bytes starting on a 16-byte divisible boundary	ICH2 (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary	Intel 82801BA PCI bridge
96 contiguous bytes starting on a 128-byte divisible boundary	LPC47M102

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH2 address aliassing.

4.3 DMA Channels

Table 13. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	FDD0 and 1
3	8 or 16 bits	Open
4	8 or 16 bits	Parallel port (for ECP or EPP) & COM2
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

4.4 PCI Configuration Space Map

Table 14. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82845 component
00	01	00	PCI to AGP bridge
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801BA ICH2 PCI to LPC bridge
00	1F	01	IDE controller
00	1F	02	USB
00	1F	03	SMBus controller
00	1F	04	USB
02	00	00	Add-in AGP adapter card
01	07	00	ATI Rage
01	0E	00	Promise ATA RAID
01	0C	00	82550 LAN#1
01	0D	00	82550 LAN#2
01	09	00	PCI bus connector 1
01	0A	00	PCI bus connector 2
01	0B	00	PCI bus connector 3

4.5 Interrupts

The interrupts can be routed through the Advanced Programmable Interrupt Controller (APIC) portion of the ICH2 component. The APIC is supported in Windows* 2000 Server and Windows XP and supports a total of 24 interrupts.

Table 15. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	MPU-401
6	FDD0
7	LPT1 (Note 1) FDD1
8	Real-time clock
9	Reserved for ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16 (Note 2)	AGP video (through PIRQA)
17 (Note 2)	User available (through PIRQB)
18 (Note 2)	(optional) (through PIRQC)
19 (Note 2)	ICH2 USB controller 1 (through PIRQD)
20 (Note 2)	On-board ATI Rage XL PCI
21 (Note 2)	(optional)/User available (through PIRQF)
22 (Note 2)	(optional)/User available (through PIRQG)
23 (Note 2)	ICH2 USB controller 2/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

4.6 PCI Interrupt Routing Map

The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either on-board or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the S845WD1-E server board and therefore share the same interrupt. Table 16 shows an example of how the PIRQ signals are routed on the S845WD1-E server board.

Using Table 16 as a reference, assume an add-in card using INTB is plugged into PCI bus connector 3. In PCI bus connector 3, INTB is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 3 now shares interrupts with these on-board interrupt sources.

Table 16. PCI Interrupt Routing Map

PCI Interrupt Source	PIRQ Assignment for Woodruff									
	A	B	C	D	E	F	G	H	IDSEL	Req/Gnt
AGP connector	A	B								
ICH2 USB controller 1				A						
SMBus controller		A								
ICH2 USB controller 2								A		
ICH2 Audio/Modem										
82550 LAN#1			A						28	1
82550 LAN#2				A					29	2
ATA RAID							A		30	3
ATI Rage					A				31	4
PCI bus connector 1		D				A	B	C	25	0
PCI bus connector 2		C				D	A	B	26	5
PCI bus connector 3		B				C	D	A	27	5

NOTE

In PIC mode, the ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 15 for the allocation of PIRQ lines to IRQ signals in APIC mode.

5. Connectors and Jumper Blocks

5.1 Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 17. Power Connector Pin-out (J2H1)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5Vdc	Red	16	PS_ON#	Green
5	COM	Black	17	COM	Black
6	+5Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR_OK	Gray	20	RSVD_(-5V)	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12Vdc	Yellow	22	+5Vdc	Red
11	+12Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

Table 18. 12V Auxiliary Power Connector (J4B1)

Pin	Signal
1	Ground
2	Ground
3	Ground
4	Ground
5	+12V
6	+12V
7	+12V
8	+12V

NOTE

The board will not boot if the 12V auxiliary power connector is not attached to the board.

5.2 PCI Bus Connectors

Table 19. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#) (See Note)	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK) (See Note)	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS) (See Note)	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI) (See Note)	B4	Not connected (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	Not connected (PRSNT1#) (See Note)	A40	SMBus Clock Line	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	SMBus Data Line	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#) (See Note)	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

Note: These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

5.3 AGP Connector

Table 20. AGP Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12 V	B1	Not connected	A34	Vddq	B34	Vddq
A2	TYPEDET#	B2	+5 V	A35	AD22	B35	AD21
A3	Reserved	B3	+5 V	A36	AD20	B36	AD19
A4	Not connected	B4	Not connected	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vddq	B40	Vddq
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V (aux)
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	Reserved	A47	STOP#	B47	Vddq
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vddq	B52	Vddq
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Reserved	B22	Reserved	A55	Ground	B55	Ground
A23	Ground	B23	Ground	A56	AD9	B56	AD10
A24	Reserved	B24	+3.3 V (aux)	A57	C/BE0#	B57	AD8
A25	Vcc3.3	B25	Vcc3.3	A58	Vddq	B58	Vddq
A26	AD30	B26	AD31	A59	AD_STB0#	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vddq	B64	Vddq
A32	AD_STB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	VRREFG_C	B66	VREFC_G

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

5.4 Front Panel Connector

A high density, 34-pin SSI header is provided to support a system front panel. The header contains reset, NMI, power control buttons, and LED indicators. The following table details the pin out of the header.

Table 21. High-Density Front Panel 34-Pin Header Pin Out (J8H4)

Pin	Signal Name	Pin	Signal Name
1	Power LED Anode	2	5VSB
3	KEY	4	Unused
5	Power LED Cathode	6	Unused
7	HDD Activity LED Anode	8	Unused
9	HDD Activity LED Cathode	10	Unused
11	Power Switch	12	NIC#1 Activity LED Anode
13	GND (Power Switch)	14	NIC#1 Activity LED Cathode
15	Reset Switch	16	I2C SDA
17	GND (Reset Switch)	18	I2C SCL
19	ACPI Sleep Switch	20	Chassis Intrusion
21	GND (ACPI Sleep Switch)	22	NIC#2 Activity LED Anode
23	Unused	24	NIC#2 Activity LED Cathode
25	KEY	26	KEY
27	Unused	28	Unused
29	Unused	30	Unused
31	Unused	32	Unused
33	Unused	34	Unused

5.5 VGA Connector

The following table details the pin out of the VGA connector.

Table 22. VGA Connector Pin-out (J3A1)

Pin	Signal Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND

6	GND
7	GND
8	GND
9	Fused VCC(+5V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

5.6 NIC /USB Connector

The S845WD1-E server board supports one Magjack3* connector (dual USB + RJ45). The following table details the pin out of the connector.

Table 23. Magjack3 Connector (dual USB + RJ45) Pin Out (JA4A1)

Pin	Signal Name	Pin	Signal Name
1	VREG_USB_BP	16	NC
2	USB_BACK1_R	17	NC
3	USB_BACK1_R	18	GND
4	GND	19	LAN_SEC_SPEED
5	VREG_USB_BP	20	I_LED2_V_P3P_PAUX
6	USB_BACK2_R	21	LAN_SEC_LINK
7	USB_BACK2_R	22	I_R_LAN_SEC_ACT
8	GND	23	GND
9	NC	24	GND
10	LAN_SEC_TDP	25	GND
11	LAN_SEC_TDN	26	GND
12	LAN_SEC_RDP	27	GND
13	LAN_SEC_RDN	28	GND
14	NC	29	GND
15	NC	30	GND

5.7 ATA Connectors

The S845WD1-E board provides two 40-pin, low-density ATA-100 RAID connectors. The pin out for both connectors is identical and is listed in the following table.

Table 24. ATA-100, 40-pin Connectors Pin Out (J8G2,J8H3)

Pin	Signal Name	Pin	Signal Name

Pin	Signal Name	Pin	Signal Name
1	RIDE_R_DRVRST	2	GND
3	RIDE_PD7	4	RIDE_PD8
5	RIDE_PD6	6	RIDE_PD9
7	RIDE_PD5	8	RIDE_PD10
9	RIDE_PD4	10	RIDE_PD11
11	RIDE_PD3	12	RIDE_PD12
13	RIDE_PD2	14	RIDE_PD13
15	RIDE_PD1	16	RIDE_PD14
17	RIDE_PD0	18	RIDE_PD15
19	GND	20	KEY
21	RIDE_PDMARQ	22	GND
23	RIDE_PIOW	24	GND
25	RIDE_PIOR	26	GND
27	RIDE_PIORDY	28	GND
29	RIDE_PDMACK	30	GND
31	RIDE_PINTRQ	32	Test Point
33	RIDE_PA1	34	RIDE_PDIAG
35	RIDE_PA0	36	RIDE_PA2
37	RIDE_PCS0	38	RIDE_PCS1
39	RAID_IDE_ACT#	40	GND

The S845WD1-E board provides two 40-pin, low-density ICH2 IDE connectors. The pin out for both connectors is identical and is listed in the following table.

Table 25. ICH2 IDE 40-pin Connector Pin Out (J5H1, J5G2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground

Pin	Signal Name	Pin	Signal Name
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Not connected
33	PDA1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	PDA0 (Address 0)	36	PDA2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

5.8 Front Panel USB Header

A header on the server board provides an option to support two additional USB connectors. The pin out of the header is detailed in the following table.

Table 26. Front Panel USB Connector Pin-out (J8G1)

Pin	Signal Name
1	USB_FNT_PWR
2	USB_FNT_PWR
3	USB_ICH_FRONT1#
4	USB_ICH_FRONT2#
5	USB_ICH_FRONT1
6	USB_ICH_FRONT2
7	GND
8	GND
9	NC
10	NET_USB_FNT_P10

5.9 Floppy Connector

The S845WD1-E server board provides a 34-pin connector interface to the floppy drive controller. The following table details the pin out of the 34-pin floppy connector.

Table 27. 34-pin Floppy Connector Pin Out (J5H2)

Pin	Signal Name	Pin	Signal Name
1	GND	2	DENSEL
3	Key	4	NC
5	Key	6	DRVDEN1
7	GND	8	FDINDX#
9	GND	10	MTR0# (Motor Enable A)
11	GND	12	NC
13	GND	14	DS0# (Drive Select A)
15	GND	16	NC
17	NC	18	DIR# (Stepper Motor Direction)
19	GND	20	STEP# (Step Pulse)
21	GND	22	WDATA# (Write Data)
23	GND	24	WGATE# (Write Enable)
25	GND	26	TRK0# (Track 0)
27	NC	28	WRTPRT# (Write Protect)
29	GND	30	RDATA# (Read Data)
31	GND	32	HDSEL# (Side 1 Select)
33	GND	34	DSKCHG# (Diskette Change)

5.10 Serial Port Connector

The S845WD1-E server board has one 9-pin D-sub serial port connector and one 2 x 5 serial port connector. The following tables detail the pin outs of these two ports.

Table 28. 9-pin Serial A Port Pin Out (J2A1)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 29. 10-pin Header Serial B Port Pin Out (J2G1)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)
10	Key

5.11 Keyboard and Mouse Connector

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch* circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

Table 30. Keyboard /Mouse PS/2 Connector Pin Out (J1A1)

Pin	Signal Name
1	Data
2	NC
3	GND
4	+5 V (Fused)
5	Clock
6	NC

5.12 Miscellaneous Headers

5.12.1 Fan Headers

The S845WD1-E server board provides four 3-pin fan headers. All fans use direct 12 volts. All fans, labeled “CPU_FAN”, “Fan1”, “Fan2” and “Fan3” are wired to a fan tachometer input of the Hardware Management ASIC.

Table 31. Three-Pin Fan Headers Pin- Out for CPU_FAN and FAN1 (CPU_FAN: J1F1, FAN1: J8H2, FAN2: J1B1, FAN3: J5H3)

Pin	Signal Name	Type	Description
1	CNTL	Power	GROUND is the power supply ground
2	VREG_12V_POWER	Power	12 V
3	Fan Tach	Out	FAN_TACH signal is connected to the Hardware Management ASIC to monitor the fan speed

5.13 System Recovery and Update Jumper

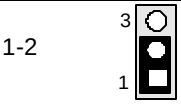
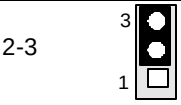
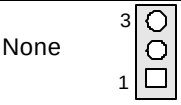
CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

This 3-pin jumper block determines the BIOS Setup program mode. Table 32 describes the jumper settings for the three modes: normal, configure, and recovery.

When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

Table 32. BIOS Setup Configuration Jumper Settings (J6H1)

Function/Mode	Jumper Setting	Configuration
Normal	1-2 	The BIOS uses current configuration information and passwords for booting.
Configure	2-3 	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None 	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 7
BIOS recovery	Section 6.6

6. BIOS Features

The S845WD1-E server board uses an Intel/AMI* BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The S845WD1-E server board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected system memory.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as WD84510A.86B.

When the S845WD1-E server board's jumper is set to configuration mode and the server is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
The S845WD1-E server board's compliance level with Plug and Play	Section 3.6.1.3

6.1 BIOS Flash Memory Organization

The Intel® 82802AB Firmware Hub (FWH) includes a 4 megabit symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

6.2 Resource Configuration

6.2.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be on-board or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

6.2.2 PCI IDE Support

If Auto is selected from the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 7.3.4.1). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.

To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the

capability of the drive. The user can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

6.3 System Management BIOS (SMBIOS)

SMBIOS is a Server Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The S845WD1-E server board's compliance level with SMBIOS	Section 6.3

6.4 Legacy USB Support

Legacy USB support enables USB devices such as keyboard, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When the user applies power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing the user to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboard and mice are recognized and may be used to configure the operating system. (Keyboard and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

Legacy USB support is for keyboard, mice, and hubs only. Other USB devices are not supported in legacy mode.

6.5 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

6.5.1 Language Support

The BIOS Setup program and help messages are supported in two languages: US English and Spanish. Additional languages may be flashed in if desired (German, Italian and French available). The default language is US English, which is present unless another language is selected in the BIOS Setup program.

6.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

6.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. The user can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Section 5.13
The Boot menu in the BIOS Setup program	Section 7.6

6.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, the ATAPI CD-ROM third, and the network fourth. The fifth device is disabled.

6.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

The network can be selected as a boot device. This selection allows booting from the on-board NIC or a network add-in card with a remote boot ROM installed.

6.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

6.8 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel Rapid BIOS

6.8.1 Intel Rapid BIOS Boot

Using the following BIOS Setup program settings reduces the POST execution time. In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup program).

For information about	Refer to
IDE Configuration Submenu in the BIOS Setup program	Section 7.3.4

6.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.

- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 33 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 33. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (See Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 7.4

7. BIOS Setup Program

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

```
Maintenance  Main      Advanced  Security  Power     Boot      Exit
```

Table 34 lists the BIOS Setup program menu features.

Table 34. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and BIS credentials and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 5.13 shows how to put the board into configuration mode.

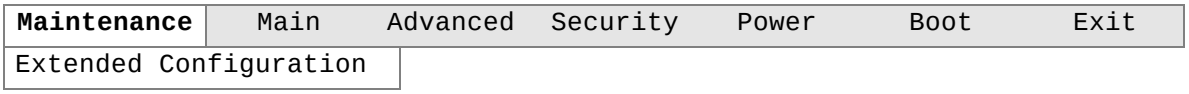
Table 35 lists the function keys available for menu screens.

Table 35. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

7.1 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.



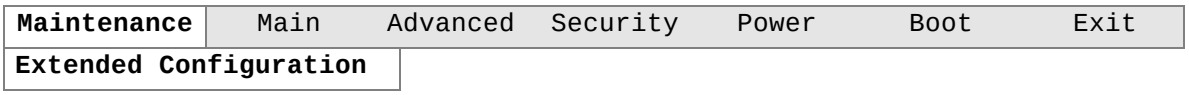
The menu shown in Table 36 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 5.13 for configuration mode setting information.

Table 36. Maintenance Menu

Feature	Options	Description
Clear All Passwords	• **Yes (default)** • No	Clears the user and supervisor passwords.
Clear BIS Credentials	• **Yes (default)** • No	Clears the Wired for Management Boot Integrity Service (BIS) credentials.
Extended Configuration	• **Default (default)** • User-Defined	Invokes the Extended Configuration submenu.
CPU Information	No options	Displays CPU Information.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.

7.1.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar and then Extended Configuration.



The submenu represented by Table 37 is for setting video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 37. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User Defined	User Defined allows setting memory control and video memory cache mode. If selected here, will also display in the Advanced Menu as: "Extended Menu: Used."
Video Memory Cache Mode	USWC **UC (default)**	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining. Selects UnCacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining.

7.2 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 38 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 38. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Hyper-Threading Technology	**Enabled (default)** Disabled	**This option is only available on the S845WD1H server board and only if an HTT enabled processor is installed.**
Processor Speed	No options	Displays processor speed.
System Bus Speed	No options	Displays the system bus speed.
Processor1 L2 Cache Size	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 1 Memory Bank 2	No options	Displays the amount and type of RAM in the memory banks.
Language	**English (default)** Español	Selects the current default language used by the BIOS (Italiano, Deutsch and Français available via .lng files).
Memory Configuration	Non-ECC **ECC (default)**	Allows the user to enable error reporting if the system and all installed memory support ECC. If non-ECC memory is installed, BIOS will detect and change the setting to Non-ECC.
Internal Cache	Disabled WriteThru **WriteBack (default)** Reserved	

Feature	Options	Description
External Cache	Disabled **WriteThru (default)** WriteBack Reserved	
IOAPIC	Disabled **Enabled (default)**	
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

7.3 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

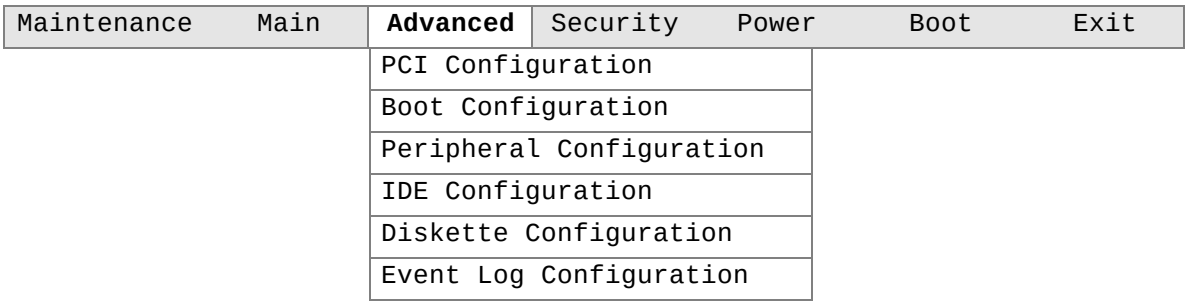


Table 39 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 39. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If Used is displayed, User-Defined has been selected in Extended Configuration under the Maintenance Menu.
PCI Configuration	Select to display submenu	Configures individual PCI slot's IRQ priority.
Boot Configuration	Select to display submenu	Configures Plug and Play and the Numlock key, and resets configuration data.
Peripheral Configuration	Select to display submenu	Configures peripheral ports and devices.
IDE Configuration	Select to display submenu	Specifies type of connected IDE devices.
Diskette Configuration	Select to display submenu	Configures the diskette drive.
Event Log Configuration	Select to display submenu	Configures event logging.

7.3.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar and then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu shown in Table 40 is used to configure the IRQ priority of PCI slots individually.

Table 40. PCI Configuration Submenu

Feature	Options	Description
PCI Slot1 IRQ Priority (Note 1)	**Auto (default)** 9 10 11	Allows selection of IRQ priority for PCI bus connector 1.
PCI Slot2 IRQ Priority (Note 1)	**Auto (default)** 9 10 11	Allows selection of IRQ priority for PCI bus connector 2.
PCI Slot3 IRQ Priority (Note 1)	**Auto (default)** 9 10 11	Allows selection of IRQ priority for PCI bus connector 3.

Notes:

1. Additional interrupts may be available if certain on-board devices (such as the serial and parallel ports) are disabled.

7.3.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

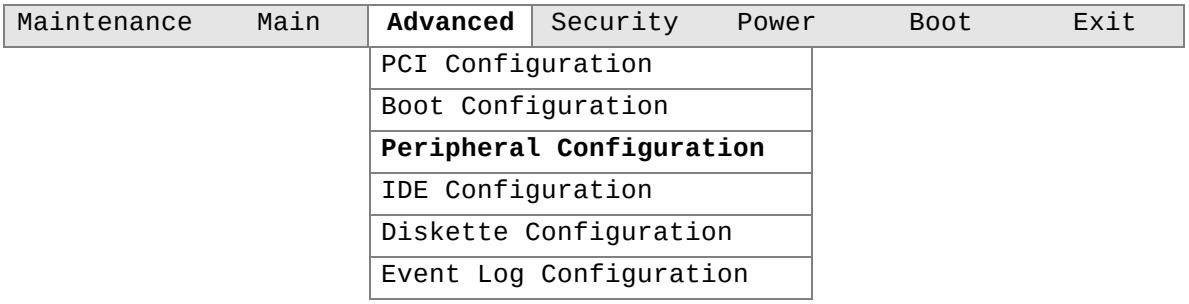
The submenu represented by Table 41 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 41. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	**No (default)** Yes	Specifies if manual configuration is desired. No lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. Yes lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Reset Config Data	**No (default)** Yes	No does not clear the PCI/PnP configuration data stored in flash memory on the next boot. Yes clears the PCI/PnP configuration data stored in flash memory on the next boot.
Numlock	Off **On** (**default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

7.3.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Peripheral Configuration.



The submenu represented in Table 42 is used for configuring computer peripherals.

Table 42. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	Disabled Enabled **Auto (default)**	Configures serial port A. Auto assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.

Feature	Options	Description
Base I/O address (This feature is present only when Serial Port A is set to Enabled)	**3F8 (default)** 2F8 3E8 2E8	Specifies the base I/O address for serial port A.
Interrupt (This feature is present only when Serial Port A is set to Enabled)	IRQ 3 **IRQ 4 (default)**	Specifies the interrupt for serial port A.
Serial Port B	Disabled Enabled **Auto (default)**	Configures serial port B. Auto assigns the first free COM port, normally COM 2, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is displayed only if Serial Port B is set to Enabled)	**2F8 (default)** 3E8 2E8	Specifies the base I/O address for serial port B.
Interrupt (This feature is displayed only if Serial Port B is set to Enabled)	**IRQ 3 (default)** IRQ 4	Specifies the interrupt for serial port B.
Mode	**Normal (default)** IrDA SIR-A ASK-IR	Specifies the mode for serial port B.
Parallel port	Disabled Enabled **Auto (default)**	Configures the parallel port. Auto assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	Output Only **Bi-directional (default)** EPP ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. Output Only operates in AT†-compatible mode. Bi-directional operates in PS/2-compatible mode. EPP is Extended Parallel Port mode, a high-speed bi-directional mode. ECP is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address (This feature is present only when Parallel Port is set to Enabled)	**378 (default)** 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to Enabled)	IRQ 5 **IRQ 7 (default)**	Specifies the interrupt for the parallel port.

Feature	Options	Description
DMA (This feature is present only when Parallel Port Mode is set to ECP)	1 **3 (default)**	Specifies the DMA channel.
Keyboard Error Message	Disabled **Enabled (default)**	Enables or disables keyboard error reporting.
LAN#1 Controller	Disabled **Enabled (default)**	Enables or disables the on-board LAN#1 device.
LAN#2 Controller	Disabled **Enabled (default)**	Enables or disables the on-board LAN#2 device.
ATA RAID Controller	Disabled **Enabled (default)**	Enables or disables the on-board ATA RAID controller.
ATI Rage Video	Disabled **Enabled (default)**	Enables or disables the on-board ATI* Rage video controller.
Legacy USB Support	Disabled **Enabled (default)**	Enables or disables Legacy USB support.

7.3.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar and then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The menu represented in Table 43 is used to configure IDE device options.

Table 43. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	Disabled Primary Secondary **Both (default)**	Specifies the integrated IDE controller. Primary enables only the primary IDE controller. Secondary enables only the secondary IDE controller. Both enables both IDE controllers.
PCI IDE Bus Master	Disabled **Enabled (default)**	Enables/disables the use of DMA for hard drive BIOS INT13 reads and writes.
Hard Disk Pre-Delay	Disabled (default) 3 Seconds 6 Seconds 9 Seconds 12 Seconds 15 Seconds 21 Seconds 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	Select to display sub-menu	Reports type of connected IDE device.
Primary IDE Slave	Select to display sub-menu	Reports type of connected IDE device.
Secondary IDE Master	Select to display sub-menu	Reports type of connected IDE device.
Secondary IDE Slave	Select to display sub-menu	Reports type of connected IDE device.

7.3.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 44 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 44. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	None User **Auto (default)** CD-ROM ATAPI Removable Other ATAPI IDE Removable	Specifies the IDE configuration mode for IDE devices. User allows capabilities to be changed. Auto fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	No options	Displays the capacity of the drive.
Multi-Sector Transfers	Disabled 2 Sectors 4 Sectors 8 Sectors **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	**Auto (default)** Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	Specifies the PIO mode.
Ultra DMA	**Disabled (default)** Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals).

7.3.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar and then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu represented by Table 45 is used for configuring the diskette drive.

Table 45. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	Disabled **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	Not Installed 360 KB, 5¼" 1.2 MB, 5¼" 720 KB, 3½" **1.44/1.25 MB, 3½" (default)** 2.88 MB, 3½"	Specifies the capacity and physical size of diskette drive A.
Floppy B	**Not Installed (default)** 360 KB, 5¼" 1.2 MB, 5¼" 720 KB, 3½" 1.44/1.25 MB, 3½" 2.88 MB, 3½"	Specifies the capacity and physical size of diskette drive B.
Diskette Write Protect	**Disabled (default)** Enabled	Disables or enables write protection for the diskette drive.

7.3.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar and then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration

The submenu represented by Table 46 is used to configure the event logging features.

Table 46. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	[Enter]	Displays the event log.
Clear All Event Logs	**No (default)** Yes	Clears the event log after rebooting.
Event Logging	Disabled **Enabled (default)**	Enables logging of events.
ECC Event Logging	Disabled **Enabled (default)**	Enables logging of ECC events.
Mark Events As Read	**Yes (default)** No	Marks all events as read.

7.4 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 47 is for setting passwords and security features.

Table 47. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	**Yes (default)** No	Clears the user password.
User Access Level (Note 2)	Limited No Access View Only **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1, Note 3, and Note 4)	**Disabled (default)** Enabled	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.
3. If both Legacy USB and Unattended Start are set to enabled in the BIOS setup menu, USB aware operating systems can unlock as PS/2 style keyboard and mouse without requiring the user to enter a password.
4. When Unattended Start is enabled in the BIOS setup menu, a USB aware operating system may override user password protection if used in conjunction with a USB keyboard and mouse without requiring the user to enter a password.

7.5 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The menu represented in Table 48 is for setting the power management features.

Table 48. Power Menu

Feature	Options	Description
ACPI	Select to display submenu	Sets the ACPI power management options.
After Power Failure	Stay Off **Last State (default)** Power On	Specifies the mode of operation if an AC power loss occurs. Stay Off keeps the power off until the power button is pressed. Last State restores the previous power state before power loss occurred. Power On restores power to the computer.
Wake on LAN	**Stay Off (default)** Power On	Specifies how the computer responds to a LAN wake up event.
Wake on PME	**Stay Off (default)** Power On	Specifies how the computer responds to a PCI power management event.
Wake on Modem Ring	**Stay Off (default)** Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.

7.5.1 ACPI Submenu

To access this menu, select Power from the menu bar at the top of the screen and then ACPI.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The submenu represented in Table 49 is for setting the ACPI power options.

Table 49. ACPI Submenu

Feature	Options	Description
ACPI Suspend State	S1 State **S3 State (default)**	Specifies the ACPI sleep state.
Wake on LAN from S5	**Stay Off (default)** Power On	In ACPI soft-off mode only, determines how the system responds to a LAN wake-up event.

7.6 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The menu represented in Table 50 is used to set the boot features and the boot sequence.

Table 50. Boot Menu

Feature	Options	Description
Quiet Boot	Disabled **Enabled (default)**	Disabled displays normal POST messages. Enabled displays OEM graphic instead of POST messages.
Intel® Rapid BIOS Boot	Disabled **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	**Disabled (default)** Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
USB Boot	Disabled **Enabled (default)**	Enables the computer to boot from USB boot devices.
PXE Remote Boot	Disabled **Enabled (default)**	Enables PXE remote boot.
Boot Device Priority	Select to display submenu	Specifies the boot sequence from the available types of boot devices.
Hard Disk Drives	Select to display submenu	Specifies the boot sequence from the available hard disk drives.
Removable Devices	Select to display submenu	Specifies the boot sequence from the available removable devices.
ATAPI CD-ROM Drives	Select to display submenu	Specifies the boot sequence from the available ATAPI CD-ROM drives.

7.6.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar and then Boot Devices Priority.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in the following table is for setting boot devices priority.

Table 51. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device 5th Boot Device	Removable Dev. Hard Drive ATAPI CD-ROM Intel UNDI, PXE-2.0 Disabled	Specifies the boot sequence according to the device type. The computer will attempt to boot from up to five devices as specified here. Only one of the devices can be an IDE hard disk drive. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The default settings for the first through fourth boot devices are, respectively: • Removable Dev. • Hard Drive • ATAPI CD-ROM • Intel UNDI, PXE-2.0

7.6.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar and then Hard Disk Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 52 is for setting hard disk drive priority.

Table 52. Hard Disk Drives Submenu

Feature	Options	Description
1st Hard Disk Drive (See Note)	Dependent on installed hard drives	Specifies the boot sequence from the available hard disk drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

7.6.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar, then Removable Devices.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 53 is for setting removable device priority.

Table 53. Removable Devices Submenu

Feature	Options	Description
1st Removable Device (Note)	Dependent on installed removable devices	Specifies the boot sequence from the available removable devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

7.6.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar and then ATAPI CD-ROM Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 54 is for setting ATAPI CD-ROM drive priority.

Table 54. ATAPI CD-ROM Drives Submenu

Feature	Options	Description
1st ATAPI CDROM (Note)	Dependent on installed ATAPI CD-ROM drives	Specifies the boot sequence from the available ATAPI CD-ROM drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CD-ROM drives, the maximum number of ATAPI CD-ROM drives supported by the BIOS.

7.7 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 55 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 55. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

8. Error Reporting and Handling

This section documents the types of system bus error conditions monitored by the S845WD1-E server board.

8.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Memory single- and multi-bit errors.
- Sensors.
- Processor internal errors, bus/address errors, thermal trip errors, temperatures and voltages, and GTL voltage levels.
- Errors detected during POST, logged as 'POST errors'.

On the S845WD1-E platform, the Heceta chip manages general hardware monitoring sensors on a hardware level; however action is only taken by software (i.e., an application such as LANDesk™ Client Manager).

8.1.1 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

8.1.2 Processor Bus Errors

The MCH supports the data integrity features supported by the Pentium® Pro bus, including address, request, and response parity. The 845E chipset always generates ECC data while it is driving the processor data bus, although the data bus ECC can be disabled or enabled by BIOS. It is enabled by default.

8.1.3 Single-Bit ECC Error Throttling Prevention

The system detects, corrects, and logs correctable errors as long as these errors occur infrequently, the system should continue to operate without a problem.

Occasionally, correctable errors are caused by a persistent failure of a single component. Although these errors are correctable, continual calls to the error logger can throttle the system, preventing further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if errors occur too frequently. Error correction remains enabled, but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure.

The BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. This entry indicates a serious hardware problem that must be repaired at the earliest possible time.

The system BIOS implements this feature for correctable bus errors. If ten errors occur within 30 minutes, the corresponding error handler disables further reporting of that type of error. The BIOS re-enables logging and SMIs the next time the system is rebooted.

8.1.4 Memory Bus Errors

The MCH is programmed to flag and log single-bit errors (SBEs) and multi-bit errors (MBEs). The MCH then triggers an SMI to the ICH2 and the ICH2 asserts the SMI# signal. BIOS then logs the errors in the event log.

8.2 BIOS Error Messages, POST Codes, and BIOS Beep Codes

The BIOS indicates the current testing phase during POST by writing a hex code to I/O location 80h. If errors are encountered, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes. POST errors are logged in to the SEL.

The error codes are defined by Intel and, whenever possible, are backward compatible with error codes used on earlier platforms.

8.2.1 BIOS Error Messages

During POST, if an error is detected, the BIOS will display an error code and message to the screen. The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are preceded by the string "Error" to highlight the fact that the system may be malfunctioning. All POST errors and warnings are logged in the SEL.

Table 56. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive A.
B: Drive Error	No response from diskette drive B.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.

Error Message	Explanation
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in on-board memory. This error is followed by an address.
Parity Error	A parity error occurred in on-board memory at an unknown address.
NVRAM/CMOS/PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

8.2.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 57 defines the uncompressed INIT code checkpoints, Table 58 describes the boot block recovery code checkpoints, and Table 59 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 57. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 58 Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 59. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.

Code	Description of POST Operation
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present.
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present.
39	Display different buses initialization error messages.
3A	New cursor position read and saved. To display the Hit <DEL> message.
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).

Code	Description of POST Operation
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.

Code	Description of POST Operation
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

8.2.2.1 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 56). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 60. BIOS Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)

8.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 61 describes the bus initialization checkpoints.

Table 61. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 62 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 62. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 63 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 63. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

9. General Specifications

9.1 Absolute Maximum Ratings

Operating an S845WD1-E baseboard at conditions, beyond those shown in the following table, may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 64. Absolute Maximum Ratings

Operating Temperature	5 degrees C to 50 degrees C [1]
Storage Temperature	-55 degrees C to +150 degrees C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:

- Chassis design must provide proper airflow to avoid exceeding the Intel® Pentium® III processor "Coppermine-T or Tualatin" maximum case temperature.
- VDD means supply voltage for the device.

9.2 S845WD1-E Power Budget

The following table shows the power consumed on each supply line for a S845WD1-E server board that is configured with one Intel Pentium 4 processor (30W max), >2 GHz FMB @ 75% usage. This configuration includes two DIMMs stacked burst at 70% maximum. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at higher-than-average stress levels.

Table 65. S845WD1-E Power Budget

Device(s)	3.3V	+5V	+12V	-12V	5V Standby	
Processors	0	0	6			
Memory DIMMs	0	4.125	0			
Server board	2.992618	1.689	0.31275	0.1	0.164612	
Fans	0	0	1.32			
Keyboard/Mouse	0	0.8	0			
PCI slots	1.909091	0.42	0			
Peripheral	4.8	5.79	5.1196			
Total Current	9.701709	12.824	12.75235	0.1	0.164612	**Total**
Total Power	32.01564	64.12	153.0282	1.2	0.823061	251.1869

9.3 Product Regulatory Compliance

9.3.1 Product Safety Compliance

The S845WD1-E complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

9.3.2 Product EMC Compliance

The S845WD1-E has been has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22, 3rd Edition (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- VCCI (Class A) – Radiated & Conducted Emissions (Japan)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI CNS13438 (Class A) Radiated & Conducted Emissions (Taiwan)
- GOST R 29216-91 (Class A) Radiated & Conducted Emissions (Russia)
- GOST R 50628-95 (Immunity) (Russia)

9.3.3 Product Regulatory Compliance Markings

This product is provided with the following product certification markings:

Product Certification Markings

UL Recognition Mark	
CE Mark	

Russian GOST Mark	ME06
Australian C-Tick Mark	N232
BSMI DOC Marking	D33025
BSMI EMC Warning	警告使用者： 這是甲類的資訊產品，在居住的環境中使用時， 可能會造成射頻干擾，在這種情況下，使用者會 被要求採取某些適當的對策
RRL MIC Mark	MIC

9.4 Electromagnetic Compatibility Notices

9.4.1 FCC (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.

- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.
All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals, that are not shielded and grounded may result in interference to radio and TV reception.

9.4.2 INDUSTRY CANADA (ICES-003)

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.
Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Apparelis Numériques", NMB-003 édictee par le Ministre Canadian des Communications.

9.4.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance to, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.4.4 Taiwan Declaration of Conformity

This product has been tested and complies with CNS13438. The product has been marked with the BSMI DOC mark to illustrate compliance.

9.4.5 Korean RRL Compliance

This product has been tested and complies with MIC Notices No. 1997-41 and 1997-42. The product has been marked with the MIC logo to illustrate compliance.

The English translation for the above is as follows:
1. Type of Equipment (Model Name): S845WD1-E
2. Certification No.: Contact Intel Representative
3. Name of Certification Recipient: Intel
4. Date of Manufacturer: Marked on Product
5. Manufacturer / Nation : Intel

9.4.6 Australia / New Zealand

This product has been tested and complies with AS/NZS 3548. The product has been marked with the C-Tick mark to illustrate compliance.

9.5 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

 WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

 ADVARSEL**!**
Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

 ADVARSEL
Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

 VARNING
Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

 VAROITUS
Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

9.6 Calculated Mean Time Between Failures (MTBF)

The MTBF (Mean Time Between Failures) for the S845WD1-E server board as configured from the factory is shown in the table below.

Product Code	Calculated MTBF	Operating Temperature
S845WD1, S845WD11U	250,008 hours	35 degrees C
S845WD1H	282,629 hours	35 degrees C

9.7 Mechanical Specifications

The following figures show the S845WD1-E server board mechanical drawings. Due to the increased thermal requirements of hyper-threading processors, the S845WD1H server board is not intended for use in a 1U form factor chassis. The S845WD11U server board is intended for use in a 1U form factor chassis and only supports up to 2.8GHz processors without hyper-threading due to thermal requirements in a 1U chassis and the thermal capabilities of the active-fan heat sink provided. If you require a 1U chassis implementation, please use the S845WD11U server board.

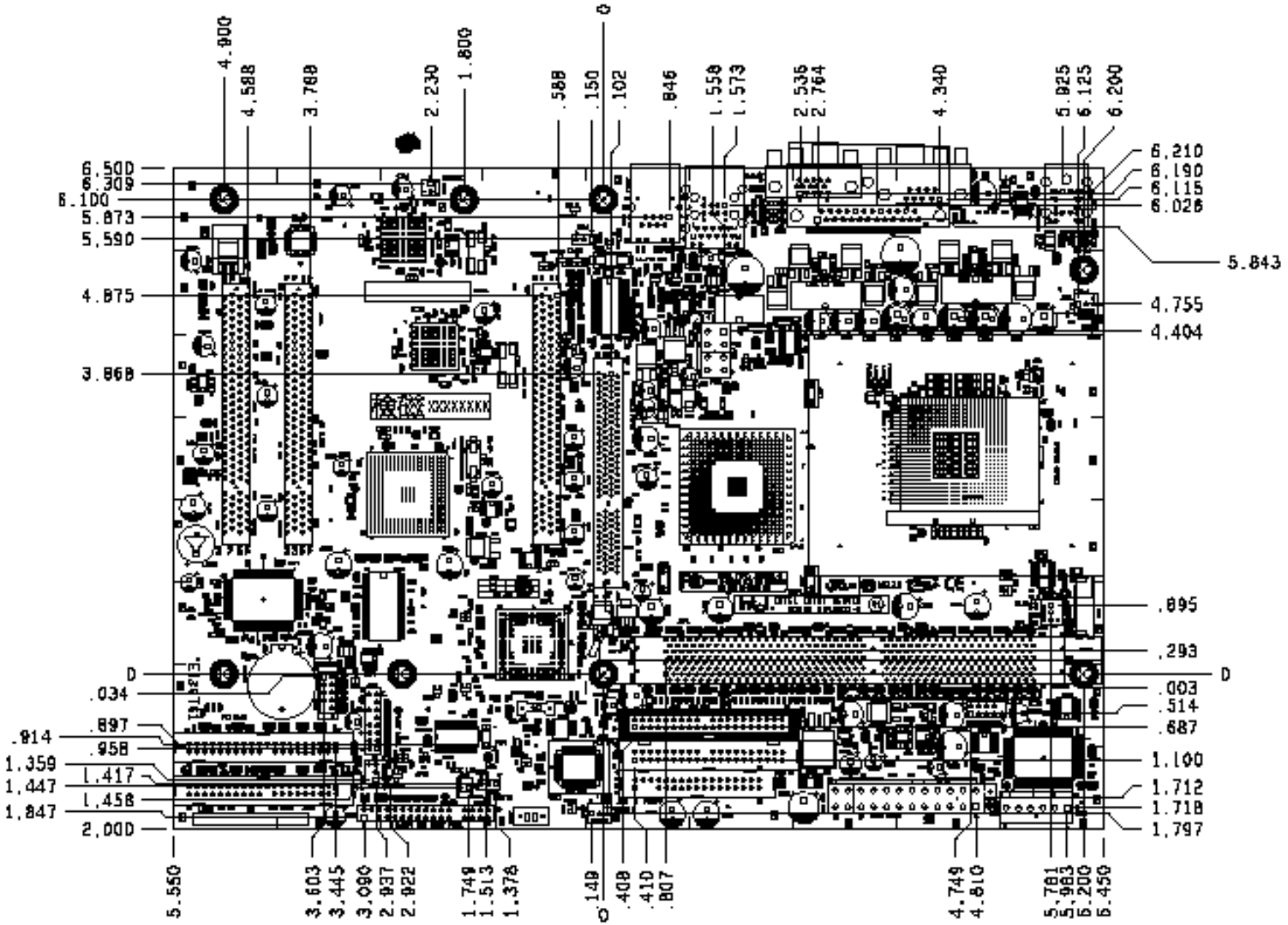


Figure 4. S845WD1, S845WD11U Server Board Mechanical Drawing

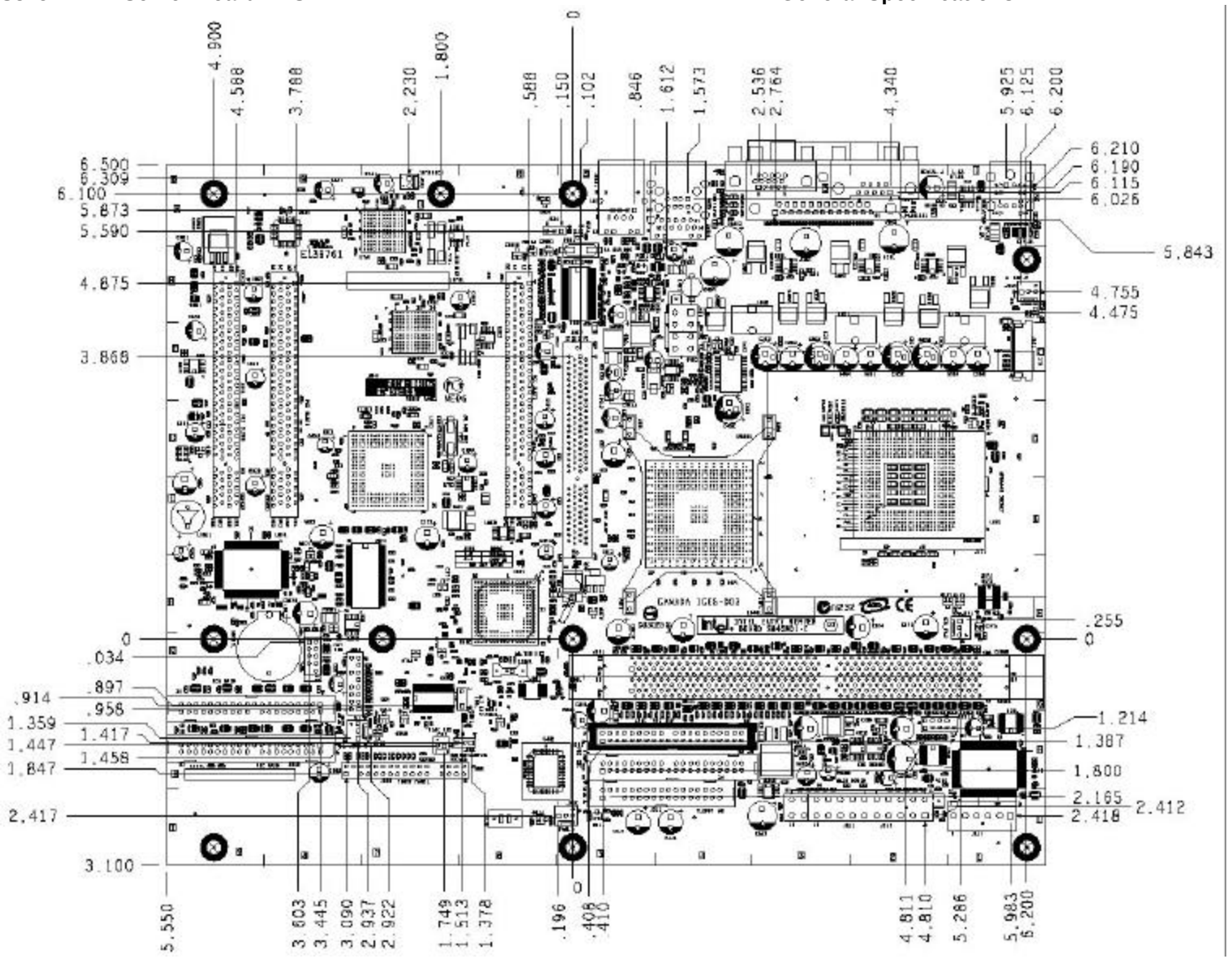


Figure 5. S845WD1H Server Board Mechanical Drawing

The following figure shows the S845WD1-E server board general purpose chassis I/O shield mechanical drawing. If the S845WD1-E server board is used in a 1U chassis, the user will need to obtain the I/O shield directly from the chassis vendor.

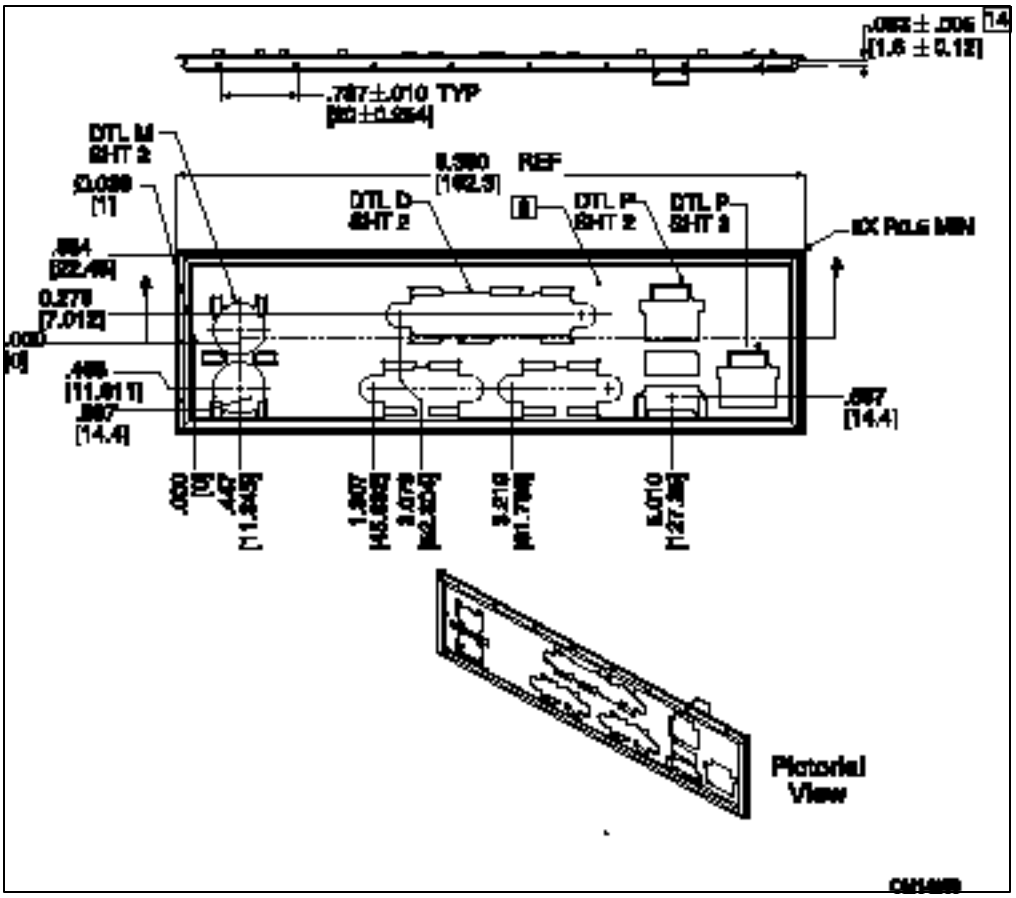


Figure 6. S845WD1-E Server Board I/O Shield Drawing

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Appendix A: S845WD1-E Integration and Usage Tips

This section provides a bullet list of useful information that is unique to the S845WD1-E server board and should be kept in mind while assembling and configuring your S845WD1-E based server.

- Only an Intel Pentium 4 or Celeron processor (in a µPGA478 socket) with a system bus of 400 /533 MHz is supported on S845WD1-E. See Section 3.1.1
- Only low profile DIMMs can be supported in a 1U server chassis.

At the completion of POST, the system status LED on the baseboard, along with the system status LED located on the front panel, will turn on green and stay on during normal operating conditions. A blinking green light or an amber light, either solid or blinking, indicates a system fault.

Appendix B: S845WD1-E Errata Listing

The following tables indicate the errata and the document changes that apply to the S845WD1-E Server Board. Intel intends to fix some of the errata in a future stepping of components, and to account for the other outstanding issues through documentation or specification changes as noted. The tables use the following notations:

Doc: Intel intends to update the appropriate documentation in a future revision.

PlanFix: Intel intends to fix this erratum in a future release of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Table 66. Errata Summary

No.	Plans	Description of Errata
1.	Fixed	BIOS Option ROM space available to adapters is 96K instead of 128K
2.	Fixed	Hard Disk Drive (HDD) LED does not always light when hard drives are attached to the IDE connectors.

Table 67. Documentation Changes

No.	Plans	Description of Documentation Change
1.	Doc	Changes to the S845WD1-E Technical Product Specification Revision 1.0
2.	Doc	Changes to the S845WD1-E Product Guide Revision 1.0.
3.	Doc	DMI and Wired for Management (WfM) information to be added to the Technical Product Specification

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.

Errata

1. BIOS Option ROM space available to adapters is 96K instead of 128K

Problem The Option ROM space available to adapters is 96K in BIOS.

Implication If using an adapter with an Option ROM greater than 32K, the onboard ATA RAID controller option ROM is disabled.

Workaround Enable Option ROMs on boot device cards only. Enabling Option ROMs on non-boot device cards can cause the available Option ROM space to run out. Drives attached to cards with their Option ROMs disabled are still available to the OS, but cannot be booted to.

Status Fixed in BIOS Production Release P03.

2. Hard Disk Drive (HDD) LED does not always light when hard drives are attached to the IDE connectors.

Problem When hard drives are attached to the primary and secondary IDE connectors, the HDD LED (indicating hard drive activity) does not always light when the S845WD1-E server board is installed in an ATX chassis.

Implication It may appear as though there is no hard drive activity due to the lack of HDD LED indications.

Status Fixed: A dual diode solution has been implemented to ensure proper LED indications.

Documentation Changes

1. Changes to the S845WD1-E Technical Product Specification Revision 1.0

Problem The following items from the S845WD1-E Technical Product Specification Revision 1.0 are incorrect and will be corrected in the next revision of the document.

Section 2.1, page 2: "2D/3D graphics controller: ATI Rage* XL Video Controller with 2MB of SDRAM." The video controller has 8MB of SDRAM.

Section 3.8.2, page 22: "The scatter/gather mechanism supports both Direct Memory Access (DMA) and Programmable I/O (PIO) IDE drives and ATAPI devices." The Promise* controller does not support ATAPI devices.

Section 3.8.2, page 22: "Support for ATA and ATAPI proposal PIO mode 0, 1, 2, 3, 4, DMA mode 0, 1, 2, and Ultra DMA Mode 0, 1, 2, 3, 4, 5." The Promise* controller does not support ATAPI devices.

Section 3.8.3.2, page 23: "The S845WD1-E supports a 2MB (512Kx32bitx4 Banks) SDRAM device for video memory." The video controller has 8MB of SDRAM.

Status Fixed: These corrections have been incorporated in revision 2.0 of the S845WD1-E Technical Product Specification.

2. Changes to the S845WD1-E Product Guide Revision 1.0

Problem The following item from the S845WD1-E Product Guide Revision 1.0 is incorrect and will be corrected in the next revision of the document.

Chapter 6, page 87: Figure 15 mislabels the main power connector on the board.

Status Fixed: These corrections have been incorporated in revision 2.0 of the S845WD1-E Product Guide.

3. DMI and Wired for Management (WfM) information to be added to the Technical Product Specification.

Problem The following information is missing from the S845WD1-E Technical Product Specification Revision 1.0 and will be added in the next revision of the document.

The S845WD1-E server board complies with DMI specification 2.0 and Wired for Management (WfM) specification 2.0.

Status Fixed: These additions have been incorporated in revision 2.0 of the S845WD1-E Technical Product Specification, Section 3.4.

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
AP	Application Processor
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BGA	Ball-grid Array
BIOS	Basic input/output system
Byte	8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DCD	Data Carrier Detect
DMA	Direct Memory Access
DMTF	Distributed Management Task Force
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
Hz	Hertz (1 cycle/second)
HDG	Hardware Design Guide
I^2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IMB	Inter Module Bus
IP	Internet Protocol
IRQ	Interrupt Request
ITP	In-target probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local area network

Term	Definition
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count
LSB	Least Significant Bit
MB	1024 KB
MBE	Multi-Bit Error
Ms	milliseconds
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
Mux	multiplexor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance
PBGA	Pin Ball Grid Array
PERR	Parity Error
PIO	Programmable I/O
PMB	Private Management Bus
PMC	Platform Management Controller
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAIDIOS	RAID I/O Steering
RAM	Random Access Memory
RI	Ring Indicate
RISC	Reduced instruction set computing
RMCP	Remote Management Control Protocol
ROM	Read Only Memory
RTC	Real Time Clock
SBE	Single-Bit Error
SCI	System Configuration Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System event log
SERIRQ	Serialized Interrupt Requests
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol

Term	Definition
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus
VGA	Video Graphic Adapter
VID	Voltage Identification
VRM	Voltage Regulator Module
Word	16-bit quantity
ZCR	Zero Channel RAID

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