

ATM2 OC12/STM4 IQ PICs (M40e Router)

Figure 1: 1-Port ATM2 OC12/STM4 IQ PIC

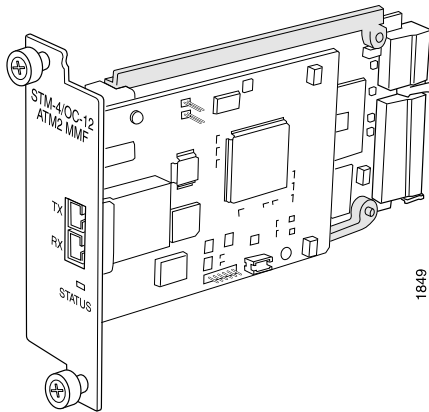
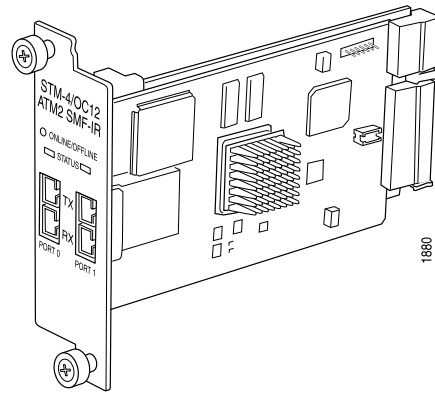


Figure 2: 2-Port ATM2 OC12/STM4 IQ PIC



Software release ■ JUNOS 5.5 and later

Description

- One or two OC12 ports
- Power requirement:
 - 1-port: 0.41 A @ 48 V (20 W)
 - 2-port: 0.52 A @ 48 V (25 W)
- Fine-grained queuing per logical interface
- Conforms to ANSI T1.105-1991 and T1E1.2/93-020R1
- Complies with ATM and SONET/SDH standards
- Alarm and event counting and detection
- Compatible with well-known ATM switches
- ATM switch ID, which displays the switch IP address and local interface name of the adjacent Fore ATM switches

Hardware features

- ATM2 IQ 1-port OC12 PICs have one 3010 SAR for segmentation and reassembly into 53-byte ATM cells; ATM2 IQ 2-port OC12 PICs have dual 3010 SAR
- High-performance parsing of SONET/SDH frames
- ASIC-based packet segmentation and reassembly (SAR) management and output port queuing
- 64 MB SDRAM memory for ATM SAR
- Packet buffering, Layer 2 parsing

Software features	<ul style="list-style-type: none"> ■ Circuit cross-connect for leveraging ATM access networks ■ User-configurable virtual circuit (VC) and virtual path (VP) support ■ Support for idle cell or unassigned cell transmission ■ OAM fault management processes alarm indication signal (AIS), remote defect indication (RDI), and loop cells ■ Point-to-point and point-to-multipoint mode Layer 2 counters per VC and per VP ■ Local and remote loopback ■ ATM Inverse ARP, which enables routers to automatically learn the IP address of the router on the far end of an ATM PVC ■ Simple Network Management Protocol (SNMP): <ul style="list-style-type: none"> ■ Management Information Base (MIB) 2 (RFC 1213) ■ ATM MIB (RFC 1695) ■ SONET MIB ■ Unspecified bit rate (UBR), non-real-time variable bit rate (VBR), and constant bit rate (CBR) traffic shaping ■ Per-VC or per-VP traffic shaping ■ Support for F4 OAM cells ■ Support for 16-bit VCI range
Cables and connectors	<ul style="list-style-type: none"> ■ Duplex SC/PC connector (Rx and Tx) ■ SONET/SDH OC12/STM4 fixed transceivers: <ul style="list-style-type: none"> ■ Intermediate Reach ■ Multimode <p>Optical interface support—See SONET/SDH OC12/STM4 Transceiver Optical Interface Specifications</p>
LEDs	<p>One tricolor per port:</p> <ul style="list-style-type: none"> ■ Off—Not enabled ■ Green—Online with no alarms or failures ■ Yellow—Online with alarms for remote failures ■ Red—Active with a local alarm; router has detected a failure

Alarms, errors, and events

- Alarm indication signal—line (AIS-L)
- Alarm indication signal—path (AIS-P)
- Bit error rate—signal degrade (BERR-SD)
- Bit error rate— signal fail (BERR-SF)
- Loss of cell delineation (LOC)
- Loss of frame (LOF)
- Loss of pointer (LOP-P)
- Loss of signal (LOS)
- Payload mismatch (PLM-P)
- Payload unequipped (unequipped STS at path level) (UNEQ-P)
- Remote defect indication—line (RDI-L)
- Remote defect indication—path (RDI-P)
- Error detection:
 - Bit interleaved parity errors B1, B2, B3
 - Errored seconds (ES-S, ES-L, ES-P)
 - Far-end bit errors, remote error indication—line (REI-L), far-end line coding violations (CV-LFE)
 - Far-end bit errors, remote error indication—path (REI-P), far-end path coding violations (CV-PFE)
 - Far-end errored seconds (ES-LFE, ES-PFE)
 - Far-end severely errored seconds (SES-LFE, SES-PFE)
 - Far-end unavailable seconds (UAS-LFE, UAS-PFE)
 - Severely errored framing (SEF)
 - Severely errored framing seconds (SEFS-S)
 - Severely errored seconds (SES-S, SES-L, SES-P)
 - Unavailable seconds (UAS-L, UAS-P)

Related Topics

- M40e Physical Interface Cards (PICs) Description
- High Availability Features (M40e Router)
- PIC Combinations (M40e Router)
- M40e PICs Supported
- FPCs Supported (M40e Router)
- PIC/FPC Compatibility (M40e Router)
- SONET/SDH OC12/STM4 Transceiver Optical Interface Specifications

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