MMS1W50-HM 200Gb/s QSFP56 FR4 Transceiver Product Specifications

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Table of Contents

Introduction 3
Key Features 3
Applications 3
Pin Description 4
QSFP56 Pin Description 4
QSFP56 Module Pad Layout 5
Control Signals 5
Diagnostics and Other Features 6
Specifications 7
Absolute Maximum Specifications 7
Operational Specifications 7
Electrical Specifications 7
Optical Specifications 8
Memory Map 10
Mechanical Specifications 10
Mechanical Dimensions 10
Label 10
Backshell Label 10
Backshell Label Legend 11
Regulatory Compliance and Classification 11
FCC Class A Notice 12
Ordering Information 13
References 14
Appendix: Optical Connector and Patch Cable 15
Optical Connector 15
Optical LC Receptacle (transceiver, front view) 15
Fiber Patch Cable 15
LC to LC Patch Cable Fiber Connections 15
Typical Look of a Single Mode LC Fiber Patch Cable 15
Document Revision History 16

Introduction

The NVIDIA® MMS1W50-HM transceiver supports link lengths of up to 2km over Single Mode Fiber with Duplex-LC UPC connector in a QSFP56 form factor, using a nominal wavelength of 1310 nm.

This transceiver complies with the CMIS4.04, QSFP MSA, IEEE 802.3bs (relevant sections) and operates according to the InfiniBand IBTA specification (see the References section for more information), and it is designed for use in 200Gb/s HDR InfiniBand applications.

The MMS1W50-HM transceiver is certified for end-to-end use in NVIDIA HDR InfiniBand systems and is required for system specifications compliance. It is also SFF-8665 compliant, i.e. it has a standard QSFP56 connector on the electrical side towards the host system, single 3.3V supply, hot pluggable, and a two-wire serial management interface.

The MMS1W50-HM transceiver has Digital Diagnostic Functions for supply voltage, laser bias current, optical transmit and receive levels with associated warning and alarm thresholds.

Rigorous qualification and production testing in NVIDIA InfiniBand systems ensures interoperability, the best performance and out-of-the-box installation experience, reliability and durability



⚠ Images are for illustration purposes only. Product labels and colors may vary.

Key Features

- Hot-pluggable QSFP56 form factor
- Supports 212.5Gb/s aggregate bit rate
- Supports up to 2km reach (OS2)
- 4x 50G PAM4 electrical interface (200GAUI-4)
- 4x 50Gb/s CWDM transmitter
- 4x 50Gb/s retimed electrical interface
- 5.5W maximum power consumption
- RoHS compliant
- 0°C to 70°C operating case temperature range
- Single 3.3V power supply
- Duplex-LC UPC receptacles
- I^2C management interface

Applications

- 200Gb/s FR4 InfiniBand HDR

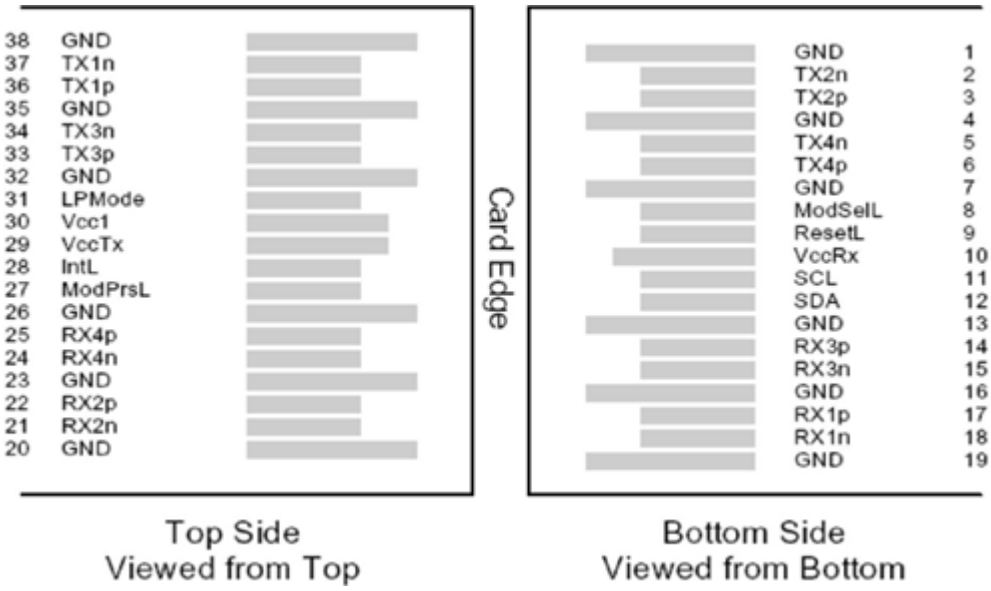
Pin Description

QSFP56 Pin Description

The transceiver's pin assignment is SFF-8679 compliant.

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Ground
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3 V Power supply receiver	29	Vcc Tx	+3.3 V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3 V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode
13	GND	Ground	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Tx3p	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

QSFP56 Module Pad Layout



Control Signals

This head end of the MCP7F60 is QSFP-Double Density and QSFP56 and the ‘tails’ are QSFP56. This means that the control signals shown in the pad layout and the pin assignments have the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Pull-up by host when no transceiver/cable is present. Connected to ground inside the transceiver. Hence, asserted low when a transceiver/cable is plugged in.
ModSelL	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum length initiates a module reset. When de-asserted the transceiver starts its initialization procedure. See the CMIS specification.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. Hardware control signal for forcing the transceiver into low-power state. Can be overwritten by low-power mode command.
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface.

Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 200 Gb/s operation.

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the CMIS 4.0 MSA.

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.
Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Relative Humidity (non-condensing)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V

Operational Specifications

This section shows the range of values for normal operation.

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature (Case)	TC	0	--	70	°C
Bit Rate (all wavelengths combined)	BR			212.5	Gb/s
Bit Error Ratio	BER			$2.4x10^{-4}$	
Reach on SMF OS1 fiber per G.652	Lmax (OS1)		--	1000	m
Reach on SMF OS2 fiber per G.652	Lmax (OS2)		--	2000	m

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Power consumption	P_D	---	---	5.5	W	
Transmitter (each lane)						
Signaling rate per lane		26.5625± 100 ppm.			Gbd	
Differential data input voltage per lane	Vin,pp,diff	900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	1
Receiver (each lane)						
Signaling rate per lane		26.5625± 100 ppm.			Gbd	

Parameter	Symbol	Min	Typical	Max	Units	Notes
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	1

Notes:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Specifications

Parameter	Min	Typical	Max	Unit	Notes
Transmitter					
Signaling rate (each lane (range)	26.5625 ± 100 ppm			GBd	
Modulation format	PAM4				
Lane wavelength (range)	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Side-mode suppression ratio (SMSR)	30			dB	
Total average launch power			10.7	dBm	
Average launch power, each lane			4.7	dBm	
Average launch power, each lane	-4.2			dBm	1
Difference in launch power between any two lanes (OMAouter) max			4	dB	
Outer Optical Modulation Amplitude (OMAouter), each lane	-1.2		4.5	dBm	2
Launch power in OMAouter minus TDECQ, each lane	-2.5			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			3.3	dB	
Average launch power of OFF transmitter, each lane			-30	dBm	
Extinction ratio	3.5			dB	

Parameter	Min	Typical	Max	Unit	Notes
RIN17.1OMA			-132	dB/Hz	
Optical return loss tolerance			17.1	dB	
Transmitter reflectance			-26	dB	3
Receiver					
Signaling rate (each lane (range)	26.5625 ± 100 ppm			GBd	
Modulation format	PAM4				
Lane wavelength (range)	1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Damage threshold, each lane	5.7			dBm	4
Average receive power, each lane			4.7	dBm	
Average receive power, each lane	-8.2			dBm	5
Difference in receive power between any two lanes (OMAouter)			4.1	dB	
Receiver reflectance			-26	dB	
Receiver sensitivity (OMAouter), each lane			-6.5	dBm	6
Stressed receiver sensitivity (OMAouter), each lane			-3.6	dBm	
Conditions of stressed receiver sensitivity test: (note 5)					
Stressed eye closure for PAM4 (SECQ), lane under test	3.3			dB	
OMAouter of each aggressor lane	0.5			dBm	
LOS De-Assert			-9	dBm	
LOS Assert	-22		-12	dBm	
LOS Hysteresis	0.5			dB	

Notes:

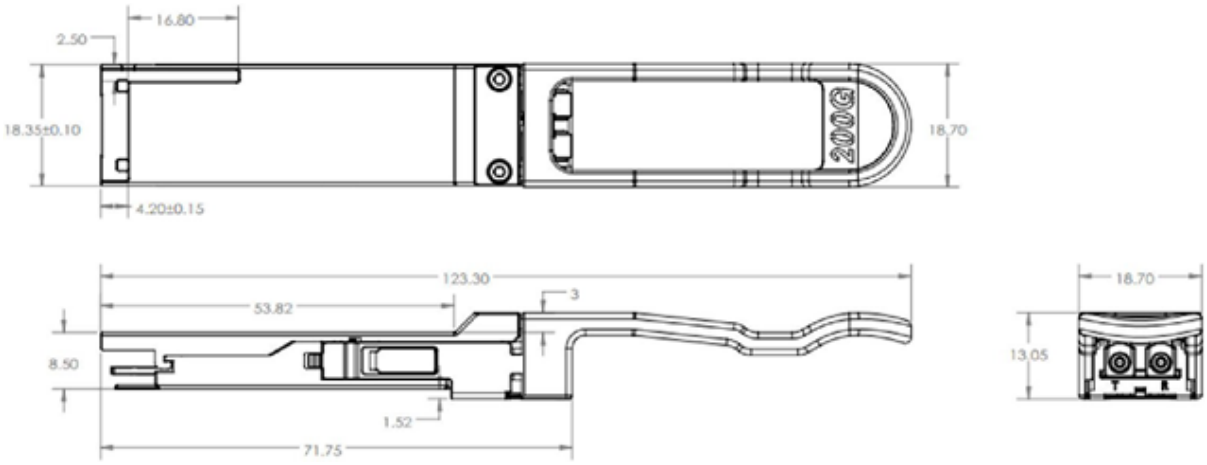
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ up to 1.4 dB.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Memory Map

The transceiver's register map is accessible as specified in CMIS 4.0 and provides information about connector type, maximum data rate, power class, part number, etc.

Mechanical Specifications

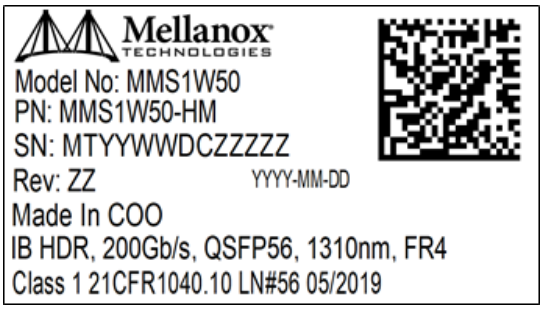
Mechanical Dimensions



Label

The following label is applied on the cable's backshell:

Backshell Label



(sample illustration)

Backshell Label Legend

Symbol	Meaning	Notes
SN - Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
XX	Manufacturer site	2 characters
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
	Quick response code	Serial number (MTYYWWXXSSSSS)

Regulatory Compliance and Classification

The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH TÜV	CDRH 21 CFR 1040 EN60950:2006 +A11+A1+A12+A2, EN60825-1:2014, EN60825-2:2004+A1+A2
Electrical Safety	TÜV UL	IEC 60950-1:2005+A1+A2 UL60950-1 (E243407)
EMC	Dekra Dekra Dekra ACMA NVIDIA	AS/NZS CISPR 32: 2013, Class A, EN55032:2012+AC:2013, Class B FCC CFR Title 47 Part 15 Subpart B: 2015, Class B CISPR 22: 2008, ANSI C63.4: 2014 ICES-003 Issue 6: 2016, Class B EN55024:2010+A1 VCCI Class B AS/NZS CISPR 32: 2013, Class A EN 55032:2012/AC2013, Class B, EN 55024:2010
Electrostatic Discharge to the Receptacle (ESD)	TÜV	IEC 61000-4-2
Robustness	NVIDIA's CM	Telcordia GR468
Environmental		EN50581: 2012 Hazardous substances REGULATION (EC) NO 1907/2006 (REACH) DIRECTIVE 2011/65/EU (2011/65/EU RoHS recast)

All versions of this laser are Class 1 laser products per IEC1/EN2 60825-1. Users should observe safety precautions such as those recommended by ANSI3 Z136.1, ANSI Z36.2 and IEC 60825-1.

FCC Class A Notice

Each of the devices complies with CFR47 FCC Class A Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur during installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by NVIDIA may void the authority granted to the user by the FCC to operate this equipment.



Ordering Information

Ordering Part Number	Description
MMS1W50-HM	Transceiver, IB HDR, up to 200Gb/s, QSFP56, LC-LC, 1310nm, FR4

References

1. SFF-8665: “QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)”, Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
    - SFF-8661
    - SFF-8679
    - SFF-8662
    - SFF-8663
    - SFF-8672
2. IEEE P802.3bs, 200GAUI-4 Interface.
3. InfiniBand HDR IBTA Specification rev 1.4: https://www.infinibandta.org/ibta-specifications-download/
4. Common Management Interface Specification (CMIS) Rev 4.0
5. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011
6. Cable and Transceiver Handling and FAQ - NVIDIA Application Note (MLNX-15-3603)
7. Measuring eye Parameters - NVIDIA Application Note (MLNX-15-5400)
8. LinkX® Memory Map – NVIDIA Application Note (MLNX-15-5926).

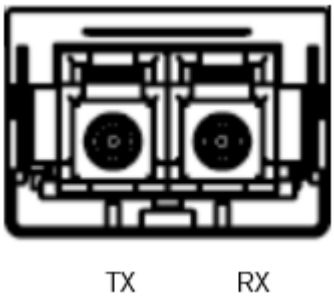
For more information, please contact your sales representative.

Appendix: Optical Connector and Patch Cable

Optical Connector

The optical port in the transceiver is a pair of LC connectors which mate with fiber-optic cables with Duplex-LC UPC connector.

Optical LC Receptacle (transceiver, front view)



Reference: IEC specification IEC 61754-20.

Fiber Patch Cable

The fiber which connects transceiver A's lane 1 must end at transceiver B's lane 12 at the other end of the link. This calls for a crossed LC cable, also referred to as 'Type B'. The fiber is standard single mode fiber. The maximum length is specified in the Operational Specifications section.

LC to LC Patch Cable Fiber Connections

Connector A Duplex LC	Connection	Connector B Duplex LC
1	--->	2
2	<---	1

Multiple LC patch cables can be connected in series, but each added connector pair adds reflections in the link which again impairs performance. An odd number of 'crosses' must be used between transceivers at the two ends.

Typical Look of a Single Mode LC Fiber Patch Cable



Document Revision History

Version	Date	Description of Change
1.3	Sep. 2023	Minor text edits.
1.2	Nov. 2021	Reformatted and rebranded; migrated to HTML. Removed BER notes.
1.1	Jul. 2021	Updated Key Features 2km reach information. Updated Operational Specifications table to include both OS1 and OS2 reach information.
1.0	Nov. 2020	First release.

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